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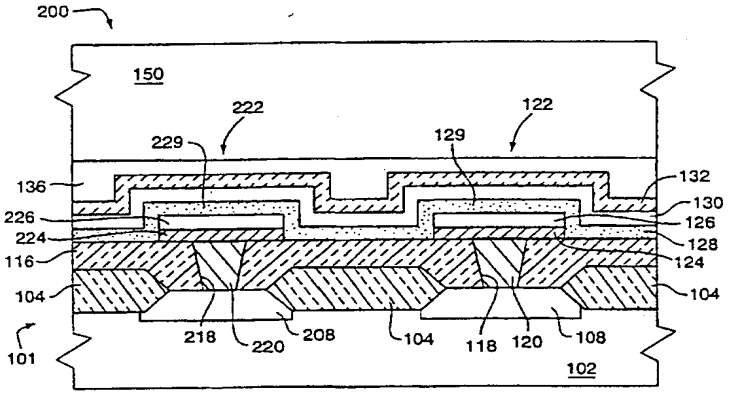

(57) Abstract: A hydrogen diffusion barrier (132, 124, 332, 324, 432, 424, 532, 524, 720, 710, 750, 770, 912) in an integrated circuit (100, 200, 300, 400, 500, 700, 740, 900) is located to inhibit diffusion of hydrogen towards a dielectric thin film (128, 328, 428, 528, 711, 764, 908) of metal oxide material. The hydrogen diffusion barrier comprises at least one of the following oxides: tantalum pentoxide; tungsten oxide; aluminum oxide; titanium oxide. The dielectric thin film is ferroelectric or high-dielectric, nonferroelectric material. Preferably, the metal oxide comprises ferroelectric layered superlattice material. The hydrogen diffusion barrier layer may be a single continuous layer (132)completely overlying a common plate electrode and the dielectric thin film, but leaving other elements in the circuit exposed to hydrogen. The dielectric thin film may be displaced laterally from transistor elements so that certain portions of the circuit remain exposed to hydrogen. A metal oxide barrier layer (124, 324, 424, 524, 710) under the dielectric film prevents diffusion of elements in the dielectric layer to the integrated circuit substrate and also acts as a hydrogen diffusion barrier layer. The hydrogen diffusion barrier layers are formed by applying a metal organic precursor solution to a substrate (102, 104, 116, 124, 126, 128 and 130) and then heating it.

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INTEGRATED CIRCUITS WITH BARRIER LAYERS AND METHODS OF FABRICATING SAME

BACKGROUND OF THE INVENTION

1. *Field of the Invention*

The invention relates to integrated circuits having barrier layers, particularly a hydrogen diffusion barrier layer to protect elements containing ferroelectric or high-dielectric constant metal oxide materials from reduction processes, and to methods of fabricating such barrier layers.

2. *Statement of the Problem*

Ferroelectric compounds possess favorable characteristics for use in nonvolatile integrated circuit memories. See Miller, U.S. Patent No. 5,046,043. A ferroelectric device, such as a capacitor, is useful as a nonvolatile memory when it possesses desired electronic characteristics, such as high residual polarization, good coercive field, high fatigue resistance, and low leakage current. Lead-containing ABO_3-type ferroelectric oxides such as lead titanate zirconate ("PZT") and lanthanum lead titanate zirconate ("PLZT") have been studied for practical use in integrated circuits. Layered superlattice material oxides have also been studied for use in integrated circuits. See Watanabe, U.S. Patent No. 5,434,102. Layered superlattice material compounds exhibit characteristics in ferroelectric memories that are orders of magnitude superior to those of PZT and PLZT compounds. Integrated circuit devices containing ferroelectric elements are currently being manufactured. Nevertheless, the persistent problem of hydrogen degradation during the manufacturing process hinders the economical production in commercial quantities of ferroelectric memories and other IC devices using ABO_3-type perovskites, layered superlattice material compounds and other metal oxide compounds having desired electronic characteristics.

A typical ferroelectric memory cell in an integrated circuit contains a semiconductor substrate and a metal-oxide semiconductor field-effect transistor ("MOSFET") in electrical contact with a ferroelectric device, usually a ferroelectric capacitor. A ferroelectric memory capacitor typically contains a thin film of ferroelectric metal oxide located between a first, bottom electrode and a second, top electrode, the

electrodes typically containing platinum. During manufacture of the circuit, the MOSFET is subjected to conditions causing defects in the silicon substrate. For example, the CMOS/MOSFET manufacturing process usually includes high energy steps, such as ion-mill etching and plasma etching. Defects also arise during heat treatment for crystallization of the ferroelectric thin film at relatively high temperatures, often in the range of 500°C - 900°C. As a result, numerous defects are generated in the single crystal structure of the semiconductor silicon substrate, leading to deterioration in the electronic characteristics of the MOSFET.

To restore the silicon properties of the MOSFET/CMOS, the manufacturing process typically includes a hydrogen annealing step, in which defects such as dangling bonds are eliminated by utilizing the reducing property of hydrogen. Various techniques have been developed to effect the hydrogen annealing, such as a forming-gas anneal ("FGA"). Conventionally, FGA treatments are conducted under ambient conditions in a H_2-N_2 gas mixture between 350°C and 550°C, typically around 400°C - 450°C, for a time period of about 30 minutes. In addition, the CMOS/MOSFET manufacturing process requires other fabrication steps that expose the integrated circuit to hydrogen, often at elevated temperatures, such as hydrogen-rich plasma CVD processes for depositing metals and dielectrics, growth of silicon dioxide from silane or TEOS sources, and etching processes using hydrogen and hydrogen plasma. During processes that involve hydrogen, the hydrogen diffuses principally through the top electrode of the memory capacitor to the ferroelectric metal oxide thin film, but also from the side edges of the capacitor, and reduces the oxides contained in the ferroelectric material. The absorbed hydrogen also metallizes the surface of the ferroelectric thin film by reducing metal oxides. As a result of these effects, the electronic properties of the capacitor are degraded. After the FGA, the remanent polarization of the ferroelectrics is very low and no longer suitable for storing information. An increase in leakage currents also results. In addition, the adhesivity of the ferroelectric thin film to the upper electrode is lowered by the chemical change taking place at the interface. Alternatively, the upper electrode is pushed up by the oxygen gas, water, and other products of the oxidation-reduction reactions taking place. Thus, peeling is likely to take place at the interface between the top electrode and the ferroelectric thin film. In addition, hydrogen also can reach the lower

electrode, leading to internal stresses that cause the capacitor to peel off its substrate. These problems are acute in ferroelectric memories containing layered superlattice material compounds because these metal oxide compounds are particularly complex and prone to degradation by hydrogen-reduction.

Several methods have been reported in the art to inhibit or reverse hydrogen degradation of desired electronic properties in ferroelectric oxide materials. Oxygen-recovery annealing at high temperature (800°C) for about one hour results in virtually complete recovery of the ferroelectric properties degraded by hydrogen treatments. However, the high-temperature oxygen-anneal itself may generate defects in silicon crystalline structure, and it may offset somewhat the positive effects of any prior forming-gas anneal on the CMOS characteristics. Also, if hydrogen reactions have caused structural damage to the ferroelectric device, such as peeling, then a recovery anneal is not able to reverse the damage effectively. Numerous other problems regarding local interconnect structures may arise from a high-temperature recovery annealing technique. Aluminum in a local interconnect has a melting point of about 660°C and begins to soften at about 450°C. Common interconnect metals, such as aluminum, copper and tungsten, are prone to excessive oxidation at higher temperatures, leading to changes in electrical conductivity and to volume expansion. Titanium nitrides are thermally unstable, and changes in electrical properties can occur as a result of high-temperature recovery annealing. Certain other materials, like copper, may migrate by diffusion through the top metal electrode of a memory capacitor into the ferroelectric metal oxide material.

To protect the ferroelectric metal oxide element by reducing the detrimental effects of backend hydrogen heat treatments, including forming gas anneals (FGAs), CVD processes and etching steps, the prior art teaches the application of hydrogen diffusion barrier layers to inhibit the diffusion of hydrogen into the ferroelectric material. The barrier layer is typically located over the ferroelectric element, but it can also be located below and laterally to the sides of the element. Hydrogen diffusion barrier layers of the prior art often give rise to problems. Titanium nitride has been mentioned for use as an electrically conductive hydrogen diffusion barrier layer. The deposition of nitride layers, however, is relatively difficult, usually requiring a sputtering method. Sputtering of a titanium target can also result in free titanium being deposited, which

may diffuse into the ferroelectric metal oxide thin film. A problem with an electrically conductive barrier layer, in general, is that it cannot be allowed to form a short circuit between layers. Thus, a conductive barrier layer is practically limited to the top surface of the top electrode of a ferroelectric capacitor, and cannot be used to cover the sides unless an insulating layer is interposed. Silicon nitride has also been mentioned as a hydrogen diffusion barrier layer. Silicon nitride is conventionally deposited using a CVD technique by reacting silane with ammonia in an argon plasma, or by reacting silane in a nitrogen discharge. However, such high-energy hydrogen-rich processes likely cause hydrogen damage to the ferroelectric metal oxide in the process of forming the hydrogen diffusion barrier layer. Also, silicon nitride is a relatively stressed material, and it is prone to formation of cracks at the higher temperatures at which some backend processes are performed.

Another ferroelectric device known in the art is a nonvolatile, nondestructive read-out ("NDRO") memory in which the memory element is a single ferroelectric field effect transistor ("ferroelectric FET"), thereby reducing some of the complexity of conventional 2T - 2C ("two-transistor - two capacitor") operation. A structure well-known in the art is the so-called metal-ferroelectric-semiconductor FET ("MFS-FET"), in which a ferroelectric layer is formed on the semiconductor substrate, and the metal gate electrode is located on the ferroelectric layer. The ferroelectric layer typically comprises a ferroelectric metal oxide similar to the metal oxides used in conventional 2T - 2C memory capacitors, and the ferroelectric layer is similarly subject to hydrogen degradation during fabrication. Also, when a ferroelectric metal oxide, such as PZT, is formed directly on a semiconductor substrate, such as silicon, high leakage current, low retention times and fatigue are common problems in a ferroelectric FET. It is commonly believed in the art that some of this is a result of a poor interface between ferroelectric oxides and silicon. The poor interface may be a result of incompatibility of crystalline ferroelectric oxides with the crystal lattices and thermal coefficients of silicon. Furthermore, when a thin film of ferroelectric oxide is in direct electrical connection with the gate oxide layer of the transistor gate, it is difficult to apply sufficient voltage to the ferroelectric thin film to switch its polarization. A ferroelectric thin film and a gate oxide may be viewed as two capacitors in series. The dielectric constant of the ferroelectric thin film (usually 100 - 1000) is much higher than the

dielectric constant of typical gate oxides (usually about 3 - 5). As a result, most of the voltage drop occurs across the low dielectric constant material, and an extra high operational voltage is required to switch the polarization of the ferroelectric thin film. This can lead to electrical breakdown of the gate oxide and other materials in the circuit. Further, a high operational voltage in excess of 3 - 5 volts would render the device incompatible with the conventional integrated circuit art. To reduce interface problems, structures have been designed in which an insulating oxide layer, such as CeO_2 or Y_2O_3, is sputter-deposited on the semiconductor substrate and the gate oxide before depositing the ferroelectric layer and gate. Such an integrated structure is referred to in the art as a metal-ferroelectric-insulator-semiconductor FET ("MFIS-FET"). It is believed that an insulator layer located on the silicon substrate between the substrate and the ferroelectric thin film avoids the problems caused by a ferroelectric-semiconductor interface. Related integrated structures, in which the ferroelectric is structurally integrated with the transistor element, contain the equivalent of a floating gate electrode located between the semiconductor and the ferroelectric, and are sometimes referred to as a metal-ferroelectric-metal-insulator-semiconductor ("MFMIS-FET") or a metal-ferroelectric-metal-semiconductor ("MFMS-FET"), depending on the presence of an insulating layer. The MFS-, MFIS-, MFMS- and MFMIS-FET and other related structurally integrated memories also share the problem with conventional memories of being structures in which the ferroelectric metal oxide is subject to degradation as a result of high temperature fabrication processes in the presence of hydrogen.

Hydrogen degradation is also a problem in complex metal oxides used in nonferroelectric, high-dielectric constant applications in integrated circuits. Hydrogen reactions cause structural damage, as described above for ferroelectric oxides, and cause degradation of dielectric properties. Examples of metal oxides subject to hydrogen degradation include: high dielectric constant, nonferroelectric AB_2O_6-type metal oxide materials, for example, $SrTa_2O_6$; barium strontium titanate ("BST"), barium strontium niobate ("BSN"), and certain other ABO_3-type perovskites; and certain layered superlattice materials. Hydrogen barrier layers are, therefore, used also to protect nonferroelectric, high-dielectric constant metal oxides. In general, measures used to avoid hydrogen degradation in nonferroelectric, high-dielectric constant metal

oxides give rise to problems similar to those described above for ferroelectric metal oxides.

In conventional memory cells containing ferroelectric or dielectric material, it is common to make a hole in an electrically nonconductive hydrogen diffusion barrier layer and fill it with local interconnect or wiring material for the purpose of providing electrical contact to an electrode of a memory capacitor. FIG. 6 shows an example of a conventional memory cell structure in which wiring layer 640 is disposed in wiring hole 639 through hydrogen diffusion barrier layer 632 and in contact with top electrode 630 of memory capacitor 622. The local interconnect or wiring material, of course, does not act as a diffusion barrier to hydrogen during an FGA or other hydrogen-containing backend process. Furthermore, during the etching process to form the hole and during the metal deposition or other process to fill the hole, hydrogen damage may occur to the underlying ferroelectric or dielectric metal oxide 628.

Thus, even when a hydrogen diffusion barrier is used, it is not uncommon for structural damage to arise in a ferroelectric or dielectric device and for hydrogen to reach the metal oxide layer and degrade the desired ferroelectric or dielectric properties of the metal oxide material. Furthermore, the problem of hydrogen degradation of ferroelectric FET memories has not been solved. Therefore, it would be useful to have new materials and structures different from those known in the art to obtain the benefits of a hydrogen barrier layer in protecting ferroelectric and dielectric oxide materials, in particular, ferroelectric layered superlattice materials, from hydrogen degradation.

SOLUTION

The invention solves the problems described above by disclosing novel compositions of material for a hydrogen diffusion barrier layer. The invention also discloses a novel method for forming a hydrogen diffusion barrier layer that avoids a hydrogen rich deposition process. In addition, the invention discloses a novel, improved structure of an integrated circuit in which a hydrogen diffusion barrier layer provides greater protection against hydrogen diffusion than conventional structures of the prior art.

A feature of the invention is a hydrogen diffusion barrier layer comprising a thin film of metal oxide selected from the group including Ta_2O_5, WO_3, Al_2O_3, and TiO_2,

preferably Ta_2O_5. The metal oxide thin film of the invention is an effective barrier to the diffusion of hydrogen. Also, because the barrier layer comprises an oxide, it acts as a "getter" of hydrogen; that is, it binds hydrogen atoms present in the barrier layer. Further, a hydrogen diffusion barrier layer of the invention is electrically nonconductive. As a result, it cannot give rise to undesired electrical shorting between layers of an integrated circuit. Thus, in one embodiment of the invention, an inventive hydrogen diffusion barrier layer may be used in direct contact with a memory capacitor to cover its sides, as well as its top electrode, thereby preventing undesired lateral diffusion of hydrogen or other elements into the ferroelectric or dielectric thin film of the capacitor. In the preferred embodiment, a Ta_2O_5 hydrogen diffusion barrier layer is in direct contact with a thin film of Ta-containing layered superlattice material, such as $SrBi_2Ta_2O_9$ or $Sr_aBi_b(Ta_cNb_d)O_{[9+(a-1)+(b-2)(1.5)]}$, where $0.9 \leq a \leq 1$, $2 \leq b \leq 2.2$, and $(c+d)=2$, and is, therefore, especially compatible with the ferroelectric metal oxide of the capacitor. In another embodiment, an inventive hydrogen diffusion barrier layer may be used to protect the ferroelectric layer of a ferroelectric FET. In this embodiment, the inventive hydrogen diffusion barrier is disposed on the top surface of the gate electrode and the sides of the ferroelectric layer, but is patterned to not cover the source and drain of the ferroelectric FET. It thereby inhibits undesired diffusion of hydrogen or other elements from above or from the sides into the ferroelectric layer, while not interfering with an FGA of the semiconductor material. In the preferred embodiment, a Ta_2O_5 hydrogen diffusion barrier layer is used to protect the ferroelectric layer. A thin film comprising an inventive metal oxide may also be used as the gate insulator, disposed between the ferroelectric layer and the semiconductor substrate, to reduce interface problems and to increase the overall dielectric constant. Preferably, the gate insulator comprises Ta_2O_5 and the ferroelectric layer is a thin film of Ta-containing layered superlattice material, such as strontium bismuth tantalate.

The invention provides a metal organic decomposition ("MOD") method of forming a metal oxide hydrogen diffusion barrier layer. The MOD method comprises preparation of a liquid metal organic precursor solution containing a metal organic precursor compound. In the preferred embodiment, the precursor solution is applied to a substrate using a liquid deposition method, such as a spin-on method or, preferably, a liquid source misted chemical deposition ("LSMCD") method. An

inventive MOD method of forming an inventive hydrogen diffusion barrier layer is less complex, more reliable and more compatible with integrated circuit structures than many conventional CVD and sputtering techniques. The metal atoms present in the precursors and deposited on the substrate are bound in metal oxide precursor compounds. Therefore, there are no free metal atoms that would be prone to migration by diffusion through other integrated circuit layers, as in many conventional CVD or sputtering techniques.

The invention further provides a novel structure of an integrated circuit in which no holes or vias are formed through a hydrogen diffusion barrier layer directly over the ferroelectric or dielectric metal oxide material being protected by the diffusion barrier. In a preferred inventive structure, the top electrode layer, the gate electrode, or other layer providing electrical contact to the dielectric or ferroelectric metal oxide, is a common plate structure, rather than a self-aligning or floating electrode associated only with a single device. An example of the inventive structure is shown in FIGS. 1 and 2, in which hydrogen diffusion barrier layer 132 is disposed on common plate top electrode 130 to cover memory capacitors 122, 222. In the exemplary structure of FIGS. 1 and 2, common plate top electrode 130 serves as top electrode for capacitors 122, 222 and other memory capacitors (not shown) in the same row (or column) of a memory array. Wiring to the top electrode of each memory capacitor is, therefore, not necessary, and there are no wiring holes through the diffusion barrier directly over the ferroelectric thin films of the memory capacitors. Similarly, in the exemplary structures depicted in FIGS. 7 and 9, common plate gate electrodes 712, 766 do not require local interconnects. Thus, there are no other holes or gaps in the hydrogen diffusion barrier layer directly over the ferroelectric (or dielectric) thin films being protected. Instead, the portions of the hydrogen diffusion barrier layer directly over the ferroelectric (or dielectric) thin films are continuous barriers against diffusion. As a result, the electrical properties of ferroelectric (or dielectric) thin film layers are less likely to be degraded by backend hydrogen-containing fabrication steps.

The composition, structure and method of the invention serve to protect a metal oxide dielectric thin film against hydrogen damage. The metal oxide material of a dielectric thin film may be ferroelectric material, or it may be nonferroelectric, dielectric material. The composition of a thin film of ferroelectric material may be selected from

a group of suitable ferroelectric oxide materials, including but not limited to: an ABO_3-type perovskite, such as a titanate (e.g., $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $PbZrTiO_3$) or a niobate (e.g., $KNbO_3$); a tungsten-bronze-type oxide; a pyrochlore-type oxide; and, preferably, a layered superlattice compound, such as strontium bismuth tantalate. Alternatively, a thin film of nonferroelectric, high-dielectric constant material may be selected from a group including, but not limited to: barium strontium titanate ("BST"), barium strontium niobate ("BSN") and certain other ABO_3-type perovskites; certain AB_2O_6-type metal oxides, including $SrNb_2O_6$, $BaTa_2O_6$, $BaNb_2O_6$ and preferably $SrTa_2O_6$; and certain layered superlattice materials.

A further feature of the invention is a lower diffusion barrier layer located between the semiconductor substrate and the device containing the ferroelectric or dielectric thin film. The lower diffusion barrier layer protects the portion of the integrated circuit below it against oxygen diffusion and metal diffusion from above. Depending on the structure of the memory cell, the lower diffusion barrier layer is electrically conductive or nonconductive. In a NDRO memory containing a ferroelectric FET, the lower diffusion barrier layer may serve as a gate insulating layer. Preferably, the lower diffusion barrier layer or a gate insulating layer comprises an inventive metal oxide material, preferably Ta_2O_5. The lower diffusion barrier layer preferably is deposited using a MOD technique.

Numerous other features, objects and advantages of the invention will become apparent from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of an integrated circuit "stacked" memory cell in accordance with a preferred embodiment of the invention in which a common plate top electrode serves as top electrode for a plurality of ferroelectric memory capacitors, and there are no wiring holes in the hydrogen diffusion barrier layer covering the memory capacitor;

FIG. 2 is a cross-sectional view perpendicular to the section depicted in FIG. 1, showing the memory capacitor of FIG. 1 and an adjacent memory capacitor, which share a common plate top electrode, and in which there are no wiring holes in the hydrogen diffusion barrier layer directly over the capacitors;

FIG. 3 is a cross-sectional view of an integrated circuit "strapped" memory cell of an alternative preferred embodiment of the invention in which a ferroelectric memory capacitor is formed above and laterally displaced from the source electrode of an FET;

FIG. 4 is a cross-sectional view of an integrated circuit "planar" memory cell of an alternative embodiment of the invention in which a memory capacitor is formed both above and laterally displaced from the source electrode of an FET;

FIG. 5 is a cross-sectional view of an integrated circuit memory cell in which a hydrogen diffusion barrier layer according to the invention covers the top and sides of the memory capacitor and a wiring hole through the hydrogen diffusion barrier layer allows electrical contact to the top electrode of the ferroelectric memory capacitor;

FIG. 6 is a cross-sectional view of a conventional integrated circuit memory cell having a wiring hole through a conventional hydrogen diffusion barrier layer;

FIG. 7 is a cross-sectional view of an integrated circuit ferroelectric FET memory cell in accordance with a preferred embodiment of the invention in which a common plate gate electrode serves as gate electrode for a plurality of ferroelectric memory capacitors, and there are no wiring holes in the hydrogen diffusion barrier layer covering the gate electrode;

FIG. 8 is a cross-sectional view of an integrated circuit ferroelectric FET memory in which a hydrogen diffusion barrier layer according to the invention covers the top and sides of the ferroelectric FET, and a local interconnect fills a wiring hole through the hydrogen diffusion barrier layer;

FIG. 9 represents another embodiment of the invention in which a ferroelectric thin film in a MFMIS-type of ferroelectric FET memory is protected by an inventive hydrogen barrier layer;

FIGS. 10A and 10B together show a flow chart showing a process flowsheet for fabricating a nonvolatile ferroelectric memory device containing a hydrogen diffusion barrier layer according to a preferred embodiment of the invention;

FIG. 11 is a cross-sectional view of an exemplary capacitor having a hydrogen diffusion barrier layer in accordance with the invention;

FIG. 12 is a graph of hysteresis curves measured before and after a FGA, in which polarization, $\mu C/cm^2$, is plotted as a function of electric field, in units of kV/cm,

in a strontium bismuth tantalate thin-film capacitor having no hydrogen diffusion barrier layer; and

FIG. 13 is a graph of hysteresis curves measured before and after a FGA, in which polarization, $\mu C/cm^2$, is plotted as a function of electric field, in units of kV/cm, in a strontium bismuth tantalate thin-film capacitor having an inventive hydrogen diffusion barrier layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

1. Overview and Description of Integrated Circuit

It should be understood that FIGS. 1 - 5, 7 - 9 depicting inventive integrated circuit devices are not meant to be actual plan or cross-sectional views of any particular portions of actual integrated circuit devices. In actual devices, the layers will not be as regular and the thicknesses may have different proportions. The various layers in actual devices often are curved and possess overlapping edges. The figures instead show idealized representations that are employed to depict more clearly and fully the structure and method of the invention than would otherwise be possible. Also, the figures represent only several of innumerable variations of dielectric and ferroelectric devices that could be fabricated using the method of the invention. FIGS. 1 - 5 depict ferroelectric memory capacitors in electrical contact with the drain of field effect transistors; but the hydrogen diffusion barrier layer of this invention can also be used in other integrated circuits having other electrical components and designs that utilize ferroelectric materials or other materials that are degraded by hydrogen. One such type of integrated circuit is a ferroelectric FET memory in which the ferroelectric element is incorporated in the switch element. An example of such a ferroelectric FET was described in McMillan, U.S. Patent No. 5,523,964 issued June 4, 1996. Exemplary structures of ferroelectric FETs made in accordance with the invention are depicted in FIGS. 7 - 9. Furthermore, although this description of the invention focuses on a hydrogen diffusion barrier layer used to protect a ferroelectric nonvolatile memory, the invention is useful to protect integrated circuit devices containing nonferroelectric metal oxide materials against hydrogen damage. For the sake of clarity, elements in FIGS. 1 - 5, 7 - 9 that are substantially similar are identified with the same reference numerals.

FIG. 1 is a cross-sectional view of an integrated circuit "stacked" memory cell

in accordance with a preferred embodiment of the invention in which a common plate top electrode serves as top electrode for a plurality of ferroelectric memory capacitors, and there are no wiring holes in the hydrogen diffusion barrier layer covering the memory capacitor. In FIG. 1, memory cell 100 is formed on a wafer 101, comprising a standard semiconductor substrate 102, preferably a p-100 silicon substrate. A field oxide region 104 is formed on a surface of semiconductor substrate 102. Semiconductor substrate 102 comprises highly doped source region 106, drain region 108 and channel region 109. A gate insulating layer 110 is formed on silicon substrate 102 between the source region 106 and drain region 108, above channel region 109. Further, a gate electrode 112 is formed on the gate insulating layer 110. Source region 106, drain region 108, channel region 109, gate insulating layer 110 and gate electrode 112 together form a MOSFET 114.

A first interlayer dielectric ("ILD") layer 116, preferably made of BPSG (boron-doped phospho-silicate glass) is located on semiconductor substrate 102 and field oxide region 104, covering MOSFET 114. ILD 116 is patterned to form vias 117, 118 to source region 106 and drain region 108, respectively. Vias 117, 118 are filled to form plugs 119, 120, respectively. Plugs 119, 120 are electrically conductive and typically comprise polycrystalline silicon or tungsten. An electrically conductive lower diffusion barrier layer 124 is located on ILD 116 in electrical contact with plug 120. Lower diffusion barrier layer 124 preferably comprises IrO_2, and typically has a thickness of from 1 nm to 30 nm, preferably from 1 nm to 5 nm.

FIG. 2 is a cross-sectional view of an integrated circuit section 200 perpendicular to the section plane depicted in FIG. 1. FIG. 2 shows memory capacitor 122 of FIG. 1 and an adjacent memory capacitor 222 from an adjacent memory cell (not shown). Memory capacitor 222 is located on plug 220, which is formed in via 218 above a drain region 208. A lower diffusion barrier layer 224 is located on plug 220. Diffusion barrier layers 124 and 224 preferably are formed simultaneously by depositing a layer of IrO_2 on ILD 116, then patterning and etching it. Bottom electrode 126 is located on lower diffusion barrier layer 124, and bottom electrode 226 is located on lower diffusion barrier layer 224. Preferably, both bottom electrodes 126, 226 are formed simultaneously by depositing a layer of platinum, preferably having a thickness of 100 nm, then patterning and etching it. Lower

diffusion barrier layers 124, 224 and bottom electrodes 126, 226 may be patterned and etched in the same series of steps. Diffusion barrier layers 124, 224 inhibit the diffusion of metal atoms and oxygen from ferroelectric thin film 128 and bottom electrodes 126, 226 into the semiconductor substrate.

As depicted in FIG. 2, ferroelectric thin film 128 is disposed on ILD 116 and bottom electrodes 126, 226. In the preferred embodiment, depicted in FIG. 2, ferroelectric thin film 128 is not etched away from the surface of ILD 116 between memory capacitors 122 and 222 because it provides extra electrical insulation to overlying common plate top electrode 130. That is, ferroelectric thin film 128 is a single, continuous dielectric layer common to both capacitors. Nevertheless, in a variation (not shown) of this embodiment, ferroelectric thin film may be removed from ILD 116 between memory capacitors 122 and 222. As shown in FIG. 1, ferroelectric thin film 128 is removed from ILD 116 in the region directly over channel region 109 and source 106 to reduce interference with FGA processes. In accordance with an important feature of the invention, a common plate top electrode layer 130, made of platinum and having a thickness of 100 nm, is formed on ferroelectric thin film 128. After patterning, common plate top electrode 130 covers the top surface of ferroelectric thin film 128. As shown in FIG. 1, however, common plate top electrode 130 does not cover ILD 116 directly over channel 109 and source 106 of MOSFET 114 in memory cell 100; nor does it cover corresponding channel and source regions of MOSFETs in memory cells aligned in the same array row (or column) as memory cell 100. Common plate top electrode 130 is patterned so that it forms stack capacitor 122 with bottom electrode 126 and ferroelectric thin film 128 when viewed in cross-section as in FIG. 1. FIG. 2 shows, however, that common plate top electrode 130 is a single continuous conducting layer providing the top electrode of memory capacitors 122, 222, as well as the top electrode of other memory capacitors aligned in the same row (or column) as memory capacitors 122, 222. A read/write voltage is applied to a memory capacitor by closing a single switch at the end of an array row (or column). The novel structure including common plate top electrode 130 allows this technique of applying a voltage bias at an end of common plate top electrode 130. Inventive hydrogen diffusion barrier layer 132 is disposed on common plate top electrode 130. Hydrogen diffusion barrier layer 132 comprises a thin film of metal oxide selected from

the group including Ta_2O_5, WO_3, Al_2O_3, and TiO_2, preferably Ta_2O_5. No wiring holes are made in hydrogen diffusion barrier layer 132. Thus, hydrogen diffusion barrier layer 132 is continuous directly over ferroelectric thin film 128. As depicted in FIG. 1, it also covers the side portion 131 of ferroelectric thin film 128. As depicted in FIG. 2, hydrogen diffusion barrier layer 132 continuously covers bottom electrode 126 and capacitor portion 129 of ferroelectric thin film 128 from directly above, as well as bottom electrode 226 and capacitor portion 229 of ferroelectric thin film 128 from directly above. Thus, the top and sides of memory capacitors 122, 222 and other capacitors (not shown) are covered by hydrogen diffusion barrier layer 132. Since the top electrode of each memory capacitor 122, 222 and others in the same row (or column) is addressed with a voltage bias applied to common plate top electrode 130, conventional electrical contacts through a hydrogen barrier layer to the top surface of each capacitor are unnecessary. As a result, the integrity of hydrogen diffusion barrier layer 132 as a hydrogen barrier is maintained. Thus, protection of ferroelectric thin film 128, in general, and capacitor portions 129, 229 of memory capacitors 122, 222, respectively, against hydrogen is better than if conventional wiring to the top of each capacitor were used. FIG. 6 shows an example of conventional wiring 640 through a hydrogen barrier layer 632 in a conventional memory cell 600.

In the preferred embodiment, ferroelectric thin film 128 comprises a thin film of ferroelectric layered superlattice material; preferably, the layered superlattice material comprises strontium, bismuth, tantalum and niobium in relative molar proportions corresponding to a stoichiometric formula $Sr_aBi_b(Ta_cNb_d)O_{[9+(a-1)+(b-2)(1.5)]}$, where $0.9 \leq a \leq 1$, $2 \leq b \leq 2.2$, and $(c+d)=2$. Preferably, $a=0.9$, $b=2.2$, and $d=0$. Alternatively, $d=0.5$. In accordance with the invention, however, ferroelectric thin film 128 may comprise other ferroelectric or nonferroelectric dielectric metal oxide materials, such as PZT or BST. Ferroelectric thin film 128 has a thickness in the range of from 5 nm to 500 nm, preferably from 30 nm to 100 nm.

Semiconductor substrate 102 may comprise silicon, gallium arsenide or other semiconductor. The bottom and top electrodes of dielectric and ferroelectric memory capacitors conventionally contain platinum. It is preferable that the bottom electrode contains a non-oxidized precious metal such as platinum, palladium, silver, and gold. In addition to the precious metal, metal such as aluminum, aluminum alloy, aluminum

silicon, aluminum nickel, nickel alloy, copper alloy, and aluminum copper may be used for electrodes of a dielectric or ferroelectric memory.

FIGS. 1 and 2 depict only one of many variations of ferroelectric and dielectric memory cells that can be fabricated using the method of the invention.

FIG. 3 is a cross-sectional view of an alternative embodiment of the invention in which a "strapped" ferroelectric memory capacitor is formed laterally displaced from the drain electrode of a MOSFET. Memory cell 300 is formed on semiconductor substrate 302, and includes field oxide areas 304, and two electrically interconnected electrical devices, a field effect transistor (MOSFET) 314, and memory capacitor 322. Transistor 314 includes a source 306, a drain 308, and a gate 312. Doped channel region 309 is located in the semiconductor substrate 302 between source 306 and drain 308. Gate insulator 310 is located on semiconductor substrate 302 above channel region 309. Gate electrode 312 is located on gate insulator 310. ILD layer 316 covers field oxide 304 and MOSFET 314, except for vias 342, 344 to source 306 and drain 308, respectively. Memory capacitor 322 includes bottom electrode 326, ferroelectric thin film 328 comprising a thin film of ferroelectric metal oxide in accordance with the invention, and common plate top electrode 330. Lower diffusion barrier layer 324 is located on ILD 316 over field oxide 304. Preferably, lower diffusion barrier layer 324 is electrically nonconductive and comprises a metal oxide selected from the group including Ta_2O_5, WO_3, Al_2O_3, and TiO_2, preferably Ta_2O_5. Memory capacitor 322 is disposed on lower diffusion barrier layer 324 over field oxide 304. Hydrogen diffusion barrier layer 332 is formed over memory capacitor 322, and then ILD 336 is formed to cover memory cell 300. Continuous hydrogen diffusion barrier layer 332, preferably containing Ta_2O_5, completely covers memory capacitor 322, except for wiring hole 348, which is made through ILD 336 and hydrogen diffusion barrier layer 332 to make contact with a portion of bottom electrode 326. Thus, the top and sides of ferroelectric thin film 328 are covered by hydrogen diffusion barrier layer 332, similar to the covering of ferroelectric thin film 128 depicted in FIGS. 1 and 2. The advantage of the variation of FIG. 3, compared to the embodiment of FIGS. 1 and 2, is that hydrogen diffusion barrier layer 332 is not directly over any portion of MOSFET 314, thereby assuring that hydrogen diffusion barrier layer 332 does not interfere with FGA processes. However, most importantly, hydrogen diffusion barrier

layer 332 is directly over ferroelectric thin film 328 and it covers side portion 331 of ferroelectric thin film 328.

FIG. 4 is a cross-sectional view of an integrated circuit memory cell of an alternative embodiment of the invention in which a memory capacitor is formed both above and laterally displaced from the source electrode of a MOSFET. It combines features of the embodiments of FIGS. 1 - 3. Electrically conductive diffusion barrier layer 424 electrically connects drain 408 of MOSFET 414 to bottom electrode 426 of memory capacitor 422. Ferroelectric thin film 428 and common plate top electrode 430 are patterned so that they are not directly over source 406, channel region 409 and drain 408 of MOSFET 414. Hydrogen diffusion barrier layer 432, preferably containing Ta_2O_5, is continuous directly over ferroelectric thin film 428, it covers the top and side of common plate top electrode 430, and it covers side portion 431 of ferroelectric thin film 428. However, hydrogen diffusion barrier layer 432 is not directly over source 406, channel region 409 and drain 408 of MOSFET 414, so it does not interfere with FGA processes.

FIG. 5 is a cross-sectional view of an integrated circuit memory cell 500 in which a hydrogen diffusion barrier layer according to the invention covers the top and sides of the memory capacitor, and a wiring hole through the hydrogen diffusion barrier layer allows electrical contact to the top electrode of the ferroelectric memory capacitor. Inventive hydrogen diffusion barrier layer 532 comprises a thin film of metal oxide selected from the group including Ta_2O_5, WO_3, Al_2O_3, and TiO_2, preferably Ta_2O_5. Hydrogen diffusion barrier layer 532 covers memory capacitor 522, including the stacked structure of lower diffusion barrier 524, lower electrode 526, ferroelectric thin film 528 and top electrode 530. Most importantly, it is directly over ferroelectric thin film 528 and covers side portion 531 of ferroelectric thin film 528. Hydrogen diffusion barrier layer 532 does not cover a surface portion 533 of top electrode 530 where wiring hole 539 is formed for wiring layer 540. Therefore, the protection against hydrogen diffusion provided to ferroelectric thin film 528 is less than provided by a structure as depicted in FIGS. 1 - 4. Nevertheless, inventive hydrogen diffusion barrier layer 532 is electrically nonconductive, so it is patterned to cover the sides of memory capacitor 522, including side 531 of ferroelectric thin film 528. Hydrogen diffusion barrier layer 532 thereby provides more protection than conventional

conductive hydrogen barriers. Furthermore, it is chemically compatible with the other structural elements of memory cell 500, and it may be formed using a MOD deposition method, instead of conventional methods for forming hydrogen diffusion barriers, such as sputtering and CVD. As a result, it provides good protection against hydrogen to ferroelectric thin film 528, without adding other problems to the fabrication and operation of memory cell 500. As explained in Example 1 below, an exemplary ferroelectric capacitor, having an inventive hydrogen diffusion barrier corresponding to the structure depicted in FIG. 5, provided very effective protection against hydrogen damage.

FIG. 7 is a cross-sectional view of an integrated circuit ferroelectric FET memory cell in accordance with a preferred embodiment of the invention in which a common plate gate electrode serves as gate electrode for a plurality of ferroelectric memory capacitors, and there are no wiring holes in the hydrogen diffusion barrier layer covering the gate electrode. In FIG. 7, ferroelectric FET memory 700 is formed on a wafer 701, comprising a standard semiconductor substrate 702, preferably a p-100 silicon substrate. A field oxide region 704 is formed on a surface of semiconductor substrate 702. Semiconductor substrate 702 comprises highly doped source region 706, drain region 708, and channel region 709. A gate insulating layer 710 is formed on silicon substrate 702 between source region 706 and drain region 708, above channel region 709. A ferroelectric thin film 711 is disposed on gate insulating layer 710. Further, a gate electrode 712 is formed on ferroelectric thin film 711. Source region 706, drain region 708, channel region 709, gate insulating layer 710, ferroelectric thin film 711, and gate electrode 712 together form a ferroelectric FET 714.

In accordance with the invention, gate electrode 712 is covered by inventive hydrogen barrier layer 720. Hydrogen barrier layer 720 covers the top of gate electrode 712 and is directly over ferroelectric thin film 711. Preferably, hydrogen barrier layer 720 also has side portions 722 that cover the side surfaces 724 of ferroelectric thin film 711. As depicted in FIG. 7, inventive hydrogen barrier layer 720 preferably covers ferroelectric FET 722 and an adjacent portion of semiconductor substrate 702. Preferably, at least portions 713 and 715 of source region 706 and drain region 708, respectively, are not covered by hydrogen barrier layer 720.

Inventive hydrogen diffusion barrier layer 720 comprises a thin film of metal oxide material selected from the group including Ta_2O_5, WO_3, Al_2O_3, and TiO_2, preferably Ta_2O_5. Gate insulating layer 710 commonly comprises silicon oxide formed by conventional means. Preferably, gate insulating layer 710 comprises an inventive hydrogen diffusion barrier layer material, which may serve as hydrogen diffusion barrier, dielectric gate insulator, and ferroelectric-semiconductor interface layer. Ferroelectric thin film 711 preferably comprises a ferroelectric layered superlattice material. Preferably, ferroelectric thin film comprises a tantalum-containing layered superlattice material, such as strontium bismuth tantalate, and gate insulating layer 710 preferably comprises Ta_2O_5.

A first interlayer dielectric ("ILD") layer 726, preferably made of BPSG (boron-doped phospho-silicate glass) is located on semiconductor substrate 702 and field oxide region 704, covering ferroelectric FET 714. ILD 726 is patterned to form vias 727, 728 to source region 706 and drain region 708, respectively. Vias 727, 728 are filled to form plugs 729, 730, respectively. Plugs 729, 730 are electrically conductive and typically comprise polycrystalline silicon or tungsten.

FIG. 8 is a cross-sectional view of an integrated circuit ferroelectric FET memory cell 740 in which a hydrogen diffusion barrier layer 750 according to the invention covers the top and sides of ferroelectric FET 744. Local interconnect 746 fills wiring hole 752 through ILD 726 and hydrogen diffusion barrier layer 750, providing electrical contact to gate electrode 712.

FIG. 9 represents another embodiment of the invention in which ferroelectric thin film 764 is protected by inventive hydrogen diffusion barrier layer 770. Integrated circuit section 760 includes ferroelectric FET 768, which is a MFMIS-type of ferroelectric memory. In ferroelectric FET 768, a metal floating electrode 762 is disposed on gate insulating layer 710 above channel region 709. Ferroelectric thin film 764 is located on floating electrode 762, and gate electrode 766, directly over ferroelectric thin film 764, is disposed on ferroelectric thin film 764. Inventive hydrogen diffusion barrier layer 770 covers gate electrode 766 and the side portions 765 of ferroelectric thin film 764.

The word "substrate" can mean the underlying wafer on which the integrated circuit is formed, such as silicon substrate 102. It may also mean any object or

surface on which a material layer is directly deposited, such as BPSG ILD 116. In this disclosure, "substrate" shall mean the object or surface to which the layer of interest is applied; for example, when we are talking about a hydrogen diffusion barrier layer, such as layer 132, the substrate on which it is deposited includes layers 102, 104, 116, 124, 126, 128 and 130, on which hydrogen diffusion barrier layer 132 is formed. The term "semiconductor substrate" refers to the initial semiconductor material and its doped regions.

Terms of orientation, such as "above", "top", "upper", "below", "bottom" and "lower" herein mean relative to semiconductor substrate 102, 302, 402, 702. For example, if a second element is "above" a first element, it means it is farther from substrate 102; and if it is "below" another element, then it is closer to substrate 102 than the other element. The long dimension of substrate 102, 302, 402, 702 defines a substrate plane that is considered to be a "horizontal" plane herein, and directions perpendicular to this plane are considered to be "vertical". The terms "over" and "directly over" are used synonymously when at least a portion of a particular layer is vertically straight above at least a portion of another layer. For example, in FIG. 1, bottom electrode 126 is directly over conductive plug 120 and a portion of drain 108. The terms "over" and "directly over" do not mean that the particular layer is in direct contact with an underlying layer. For example, the hydrogen diffusion barrier layer of the invention typically does not contact the top surface of the ferroelectric (or dielectric) layer it is protecting. As long as a hydrogen diffusion barrier layer is over a portion of a ferroelectric or dielectric layer, it protects that portion from hydrogen degradation. Similarly, the word "overlying" means that the overlying element is further from the substrate than the underlying element. It is a feature of the integrated circuit structures shown in FIGS. 1 and 2 that hydrogen diffusion barrier layer 132 completely overlies dielectric layer 128. In this disclosure and the claims, the term "completely overlying" means that the overlying element has a first end that extends away from the center of the overlying element at least up to a line perpendicular to the plane of substrate 102 and aligned with one end of the underlying element and a second end that extends away from the center of the overlying element in the opposite direction at least up to a line perpendicular to the plane of substrate 102 and aligned with the other end of the underlying element. An important part of the term "completely

overlying" is the fact that the completely overlying element overlies the entire underlying element; that is, no part of the underlying element is not overlaid by the completely overlying element. In accordance with the invention, protection is increased if a hydrogen diffusion barrier layer covers the sides of a memory capacitor or other dielectric element, thereby inhibiting lateral diffusion of hydrogen into the metal oxide material of the dielectric thin film. The term "on" is often used in the specification when referring to the deposition or formation of an integrated circuit layer onto an underlying substrate or layer. In contrast to "over", "directly over", and "overlying", the terms "on" and "onto" generally signify direct contact, as is clear in the various contexts in which it is used.

A ferroelectric thin film according to the invention typically comprises a relatively flat thin film of ferroelectric material. The terms "lateral" or "laterally" refer to the direction of the flat plane of the thin film. In FIG. 1, the lateral direction would be the horizontal direction. The vertical direction is normal, or perpendicular, to the horizontal direction. It is clear that ferroelectric elements can be fabricated with varying orientations relative to the horizontal and vertical. For example, if the ferroelectric thin film is in the vertical plane, then the word "lateral" would refer to the vertical direction, and "directly over" would refer to an orientation normal to the vertical plane of the thin film.

The term "thin film" is used herein as it is used in the integrated circuit art. Generally, it means a film of less than a micron in thickness. The thin films disclosed herein are in all instances not more than 0.5 microns in thickness. Preferably, the inventive hydrogen diffusion barrier layers are 1 nm to 200 nm thick, and most preferably 5 nm to 80 nm thick. These thin films of the integrated circuit art should not be confused with the layered capacitors of the macroscopic capacitor art which are formed by a wholly different process which is incompatible with the integrated circuit art.

When a portion of a hydrogen diffusion barrier layer or other layer is described with the term "continuous" and related terms, it means there are no holes (e.g., wiring holes) or gaps in that portion of the layer. For example, it is an important feature of the invention that portions of the inventive hydrogen diffusion barrier are continuous directly over the ferroelectric (or dielectric) thin films being protected.

Ferroelectric material is also dielectric material. The metal oxide material of a dielectric thin film may be ferroelectric material, or it may be nonferroelectric, dielectric material. The term "dielectric" used herein, in particular in the claims, may refer to either a ferroelectric material or to a nonferroelectric, dielectric material. Nevertheless, in the description, the two types are usually designated separately as "ferroelectric" and "dielectric". The composition of a thin film of ferroelectric material may be selected from a group of suitable ferroelectric oxide materials, including but not limited to: an ABO_3-type perovskite, such as a titanate (e.g., $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $PbZrTiO_3$) or a niobate (e.g., $KNbO_3$); a tungsten-bronze-type oxide; a pyrochlore-type oxide; and, preferably, a layered superlattice compound. Alternatively, a thin film of nonferroelectric, high-dielectric constant material may be selected from a group including, but not limited to: barium strontium titanate ("BST"), barium strontium niobate ("BSN"), certain ABO_3-type perovskites, and certain layered superlattice materials.

United States Patent No. 5,519,234 issued May 21, 1996 to Carlos A. Paz de Araujo et al. discloses that layered superlattice compounds, such as strontium bismuth tantalate, have excellent properties in ferroelectric applications as compared to the best prior materials and have high dielectric constants and low leakage currents. United States Patents Nos. 5,434,102 issued July 18, 1995 to Watanabe et al., and 5,468,684 issued November 21, 1995, to Yoshimori et al. describe processes for integrating these materials into practical integrated circuits.

The layered superlattice materials may be summarized generally under the formula:

(1) $A1_{w1}^{+a1}A2_{w2}^{+a2}...Aj_{wj}^{+aj}S1_{x1}^{+s1}S2_{x2}^{+s2}...Sk_{xk}^{+sk}B1_{y1}^{+b1}B2_{y2}^{+b2}...Bl_{yl}^{+bl}Q_z^{-q}$,

where A1, A2...Aj represent A-site elements in the perovskite-like structure, which may be elements such as strontium, calcium, barium, bismuth, lead, and others; S1, S2...Sk represent superlattice generator elements, which usually is bismuth, but can also be materials such as yttrium, scandium, lanthanum, antimony, chromium, thallium, and other elements with a valence of +3; B1, B2...Bl represent B-site elements in the perovskite-like structure, which may be elements such as titanium, tantalum, hafnium, tungsten, niobium, zirconium, and other elements; and Q represents an anion, which generally is oxygen but may also be other elements, such

as fluorine, chlorine and hybrids of these elements, such as the oxyfluorides, the oxychlorides, etc. The superscripts in formula (1) indicate the valences of the respective elements; for example, if Q is oxygen, then q=2. The subscripts indicate the number of moles of the material in a mole of the compound, or in terms of the unit cell, the number of atoms of the element, on the average, in the unit cell. The subscripts can be integer or fractional. That is, formula (1) includes the cases where the unit cell may vary uniformly throughout the material; for example, in $Sr_{.75}Ba_{.25}Bi_2Ta_2O_9$, 75% of the A-sites are occupied by strontium atoms, and 25% of the A-sites are occupied by barium atoms. If there is only one A-site element in the compound, then it is represented by the "A1" element and w2...wj all equal zero. If there is only one B-site element in the compound, then it is represented by the "B1" element, and y2...yl all equal zero, and similarly for the superlattice generator elements. The usual case is that there is one A-site element, one superlattice generator element, and one or two B-site elements, although formula (1) is written in the more general form since the invention is intended to include cases where either of the sites and the superlattice generator can have multiple elements. The value of z is found from the equation:

(2) $(a1w1 + a2w2...+ajwj) + (s1x1 + s2x2...+skxk) + (b1y1 + b2y2...+ blyl) = qz.$

Formula (1) includes all three of the Smolenskii type compounds discussed in United States Patent No. 5,519,234 issued May 21, 1996 referenced above. The layered superlattice materials do not include every material that can be fit into formula (1), but only those which spontaneously form themselves into crystalline structures with distinct alternating layers.

The term "stoichiometric" herein may be applied to both a solid film of a material, such as a layered superlattice material, or to the precursor for forming a material. When it is applied to a solid thin film, it refers to a formula which shows the actual relative amounts of each element in a final solid thin film. When applied to a precursor, it indicates the molar proportion of metals in the precursor. A "balanced stoichiometric" chemical formula is one in which the relative molar proportions of the elements correspond to a particular type of molecular or crystalline compound. In a balanced stoichiometric formula for a solid crystalline compound, there is just enough of each element to form a complete crystal structure of the material with all sites of the

crystal lattice occupied, though in actual practice there always will be some defects in the crystal at room temperature. For example, both $SrBi_2(TaNb)O_9$ and $SrBi_2(Ta_{1.44}Nb_{0.56})O_9$ are balanced stoichiometric formulae. In contrast, a precursor for strontium bismuth tantalum niobate in which the molar proportions of strontium, bismuth, tantalum, and niobium are 1, 2.18, 1.44, and 0.56, respectively, is represented herein by the "unbalanced stoichiometric" formula $SrBi_{2.18}(Ta_{1.44}Nb_{0.56})O_9$, since it contains excess bismuth beyond what is needed to form a complete crystalline material. The general term "stoichiometric", therefore, may refer to either a balanced or an unbalanced stoichiometric formula. In this disclosure, an "excess" amount of a metallic element means an amount greater than required to bond with the other metals present to make the desired material, with all atomic sites occupied and no amount of any metal left over.

It is known in the art that a layered superlattice material made from a precursor with an amount of superlattice generator element or B-site element in excess of the stoichiometrically balanced amount is more resistant to degradation by hydrogen than material made from a precursor containing amounts of metal corresponding to a balanced stoichiometric formula. For example, amounts in the precursor of at least one metal, such as bismuth and niobium, above or in addition to that present in a balanced formula, inhibit hydrogen degradation.

It is also known in the art that ferroelectric nonvolatile memories possessing good electronic properties are fabricated by forming a thin film of strontium bismuth tantalate material comprising chemical elements in proportions approximately represented by the stoichiometric formula $SrBi_2Ta_2O_9$.

2. Detailed Description of the Fabrication Process

The general manufacturing steps for fabricating integrated circuits containing MOSFETs and ferroelectric capacitor elements are described in Mihara, U.S. Patent No. 5,466,629 and Yoshimori, U.S. Patent No. 5,468,684. General fabrication methods have been described in other references also.

A feature of the method of the invention is the use of metal organic deposition ("MOD") precursors and MOD techniques for forming hydrogen diffusion barrier layers and dielectric thin films according to the invention. The preferred composition of the electrically nonconductive hydrogen diffusion barrier layer of the invention includes

tantalum pentoxide corresponding to the stoichiometric formula Ta_2O_5. The preferred final precursor is prepared by diluting a solution of tantalum 2-ethylhexanoate in xylenes or n-octane solvent with n-butyl acetate to 0.14 molar concentration. The composition of the inventive metal organic liquid precursor solutions and oxide layers avoids the generation of free metal atoms that could diffuse to other parts of the integrated circuit, causing damage.

It is understood that the inventive method may be used to fabricate conductive and nonconductive metal oxide diffusion barrier layers having compositions different from the preferred composition described here. Similarly, the inventive composition of precursor may be varied to form metal oxides with a composition different from the preferred composition.

Metal organic liquid precursors according to the invention can be manufactured reliably. Their composition can be easily controlled and varied, if necessary. They can be safely stored for long periods, up to six months. They are relatively nontoxic and nonvolatile, compared to precursors of the prior art. Metal oxide thin film layers formed in accordance with the invention have smooth, continuous and uniform surfaces, especially compared to oxide layers of the prior art. They can be reliably fabricated to have thicknesses in the range of 5 nm to 500 nm, maintaining important structural and electrical characteristics.

The word "precursor" used herein can mean a solution containing one metal organic solute that is mixed with other precursors to form intermediate precursors or final precursors, or it may refer to a final liquid precursor solution, that is, the solution to be applied to a particular surface during fabrication. In this disclosure, the first type of precursor is usually referred to as an "initial precursor" or designated specifically, for example, a "tantalum oxide precursor". The precursor as applied to the substrate is usually referred to as the "final precursor", "precursor mixture", or simply "liquid precursor". In any case, the meaning is clear from the context. The composition of a precursor may be described in two ways. The actual dissolved metal organic precursor compounds (solutes) and solvents and concentrations may be specified; or, for the sake of clarity, the stoichiometric formula representing the composition of the final oxide compound to be formed with the precursor may be specified.

Individual MOD precursor compounds for fabricating hydrogen diffusion barrier

layers, ferroelectric and dielectric thin films, and lower diffusion barrier layers may be selected from the group including metal beta-diketonates, metal polyalkoxides, metal dipivaloylmethanates, metal cyclopentadienyls, metal alkoxycarboxylates, metal carboxylates, metal alkoxides, metal ethylhexanoates, octanoates, and neodecanoates. Preferably, the metal precursor compound comprises a metal 2-ethylhexanoate, which is well suited for use in a LSMCD technique. The ethylhexanoates and other metalorganic precursor compounds may be stored for periods of several months when dissolved in xylenes or n-octane. A solution of tantalum ethylhexanoate is preferred for forming Ta_2O_5. Individual MOD precursor compounds are formed, for example, by interacting each of the metals of a desired compound, for example, tantalum for the hydrogen diffusion barrier layer compound, and strontium, bismuth, tantalum and niobium for the ferroelectric compound, or an alkoxide of the metal, with a carboxylic acid, or with a carboxylic acid and an alcohol, and dissolving the reaction product in a solvent. Carboxylic acids that may be used include 2-ethylhexanoic acid, octanoic acid, and neodecanoic acid, preferably 2-ethylhexanoic acid. Alcohols that may be used include 2-methoxyethanol, 1-butanol, 1-pentanol, 2-pentanol, 1-hexanol, 2-hexanol, 3-hexanol, 2-ethyl-1-butanol, 2-ethoxyethanol, and 2-methyl-1-pentanol, preferably 2-methoxyethanol. Solvents that may be used include xylenes, n-octane, 2-methoxyethanol, n-butyl acetate, n-dimethylformamide, 2-methoxyethyl acetate, methyl isobutyl ketone, methyl isoamyl ketone, isoamyl alcohol, cyclohexanone, 2-ethoxyethanol, 2-methoxyethyl ether, methyl butyl ketone, hexyl alcohol, 2-pentanol, ethyl butyrate, nitroethane, pyrimidine, 1, 3, 5 trioxane, isobutyl isobutyrate, isobutyl propionate, propyl propionate, ethyl lactate, n-butanol, n-pentanol, 3-pentanol, toluene, ethylbenzene, 1-butanol, 1-pentanol, 2-pentanol, 1-hexanol, 2-hexanol, 3-hexanol, 2-ethyl-1-butanol, 2-ethoxyethanol, and 2-methyl-1-pentanol, as well as many others. The metal, metal alkoxide, acid, and alcohol react to form a mixture of metal-alkoxocarboxylate, metal-carboxylate and/or metal-alkoxide, which mixture is heated and stirred as necessary to form metal-oxygen-metal bonds and boil off any low-boiling point organics that are produced by the reaction. Initial MOD precursors are usually made or bought in batches prior to their use; the final precursor mixtures are usually prepared immediately before application to the substrate. Final preparation steps typically

include mixing, solvent exchange, and dilution. When using a liquid deposition technique, for example, LSMCD, a metal 2-ethylhexanoate is a preferred precursor compound because the ethylhexanoates are stable in solution, have a long shelf life, form smooth liquid films, and decompose smoothly on a substrate.

Terms such as "heating", "drying", "baking", "rapid thermal process" ("RTP"), "annealing", and others all involve the application of heat. For the sake of clarity, the various terms are used to distinguish certain techniques and method steps from one another. Nevertheless, it is clear that similar techniques may be used to accomplish differently named process steps; for example, drying, baking and annealing typically may be accomplished using the same apparatus, the only differences being their function and position in a fabrication sequence, or the particular temperatures used. As a result, it would be possible to designate an annealing step as a heating step, or a drying step as a baking step. To avoid confusion, therefore, the general term "heating" may also be used to describe a fabrication step, especially in the claims describing the invention. It is further understood that one skilled in the art may accomplish a desired process result using heat as disclosed herein, while referring to the process with a term different from the one used herein.

FIGS. 10A and 10B together form a flow chart showing the steps of a generalized liquid source deposition process 800 for fabricating a hydrogen diffusion barrier layer in a ferroelectric memory cell in accordance with an embodiment of the invention. The fabrication methods, precursors and compositions disclosed herein are discussed in relation to the structure of memory capacitors 122, 222, depicted in FIGS. 1 and 2. It is understood, however, that the useful features of the invention can be applied in many variations of the generalized fabrication methods disclosed herein.

In step 810, a semiconductor wafer comprising a silicon semiconductor substrate 102 is cleaned to remove contaminants, preferably by dipping the wafer into H_2SO_4 for 30 minutes. Then the wafer is dipped into 10:1 BOE for five minutes, which removes any natural oxide that may have formed on the wafer. In step 812, field oxide 104 is grown in a furnace, preferably to a thickness of 500 nm. In step 814, source region 106, drain region 108 and channel region 109 are then formed by a conventional doping method. This includes the usual photo resist, etching and strip steps for removal of the field oxide, followed preferably by a phosphorous diffusion

step. Preferably, the doping of channel region 109 is in the range of 2×10^{15} to 10^{17} atoms/cm^3, and most preferably in the range of 10^{16} to 10^{17} atoms/cm^3, which provides a resistance of about 1 ohm to 5 ohms. Preferably, the doping of the source/drain regions 106, 108 is in the range of 10^{19} to 10^{20} atoms/cm^3. Using conventional processes, a thin gate oxide 110 is then formed followed by the formation of gate 112, preferably polysilicon, to complete the MOSFET 114.

In step 816, first interlayer dielectric ("ILD") layer 116, preferably made of BPSG (boron-doped phospho-silicate glass) is deposited by a conventional spin-on technique on semiconductor substrate 102 and field oxide region 104, to cover MOSFET 114. In step 818, ILD 116 is patterned using conventional techniques to form vias 117, 118 to source region 106 and drain region 108, respectively. In step 820, vias 117, 118 are filled using conventional techniques to form plugs 119, 120, respectively. Plugs 119, 120 are electrically conductive and typically comprise polysilicon or tungsten.

Next, a layer of electrically conductive diffusion barrier material, preferably IrO_2, is deposited on ILD 116 in electrical contact with plugs 120, 220. The material may be deposited using a conventional sputtering technique. In the preferred method, however, a conductive oxide is formed using MOD precursors. Since a very thin film thickness is desired, in the range of 1 nm to 30 nm, it is preferable to form the layer of diffusion barrier layer material using a MOD precursor and a LSMCD technique. In step 822, a final MOD precursor for a layer of electrically conductive diffusion barrier material is prepared. An initial precursor comprising a solution of iridium 2-ethylhexanoate in xylenes is diluted to 0.14 molar concentration using n-butyl acetate solvent. In step 824, wafer 101 is placed into a misted deposition reactor, and then the precursor is misted and flowed into the reactor, where it forms a liquid coating on the substrate. In step 826, the substrate and liquid coating are treated to form the layer of IrO_2. Treating may comprise a process selected from the group including: exposing to vacuum, exposing to ultraviolet radiation, drying, heating, baking, rapid thermal processing, and annealing. Treatment in step 826 typically includes drying, rapid thermal processing ("RTP"), and annealing. Drying is typically performed for one minute at 160°C, then at 260°C for four minutes. If used, the RTP is typically done at 725°C for 30 seconds, with a 100°C/sec. ramping rate. A furnace anneal,

preferably in an oxygen atmosphere, crystallizes the metal oxide compound. Annealing is preferably conducted for 60 minutes at 800°C in oxygen flowing at 5 l/m, with 10 minutes "push" and 10 minutes "pull". The conductive lower diffusion barrier layer has a thickness of from 1 nm to 30 nm, preferably about 5 nm.

Next, a layer of bottom electrode material is deposited by a conventional sputtering technique to cover the lower diffusion barrier material. Preferably, a layer of platinum having a thickness of 100 nm is formed, preferably by sputtering. In step 830, the lower diffusion barrier layer and the bottom electrode layer are patterned and etched to form lower diffusion barrier layers 124, 224 underlying bottom electrodes 126, 226, respectively.

Next, as depicted in FIG. 2, ferroelectric thin film 128 is deposited on ILD 116 and bottom electrodes 126, 226. Ferroelectric thin film 128 is deposited using a liquid source deposition method, preferably LSMCD. A misted deposition process is described in United States Patent No. 5,456,945, issued Oct. 10, 1995, to McMillan et al. Other methods of applying a liquid to a substrate, such as a spin-on method, may also be used. In step 832, a final MOD precursor for ferroelectric thin film 128 is prepared. Preferably, the final precursor contains metal organic precursor compounds in relative molar proportions corresponding to the stoichiometric formula $Sr_aBi_b(Ta_cNb_d)O_{[9+(a-1)+(b-2)(1.5)]}$, where $0.9 \leq a \leq 1$, $2 \leq b \leq 2.2$, and $(c + d) = 2$. Preferably, $a=0.9$, $b=2.2$, and $d = 0$. Alternatively, $d=0.5$. Typically, commercially available precursor solutions in which the metal precursor compounds are dissolved in xylenes are diluted with n-butyl acetate just prior to use. The preferred precursor solution contains bismuth 2-ethylhexanoate, strontium 2-ethylhexanoate, and tantalum 2-ethylhexanoate, and it is diluted in step 832 to 1.2 molar concentration with n-butyl acetate.

In step 834, wafer 101 is placed into a misted deposition reactor, and then the precursor is misted and flowed into the reactor, where it forms a liquid coating on the substrate. In step 836, the substrate and liquid coating are treated to form the layer of ferroelectric material 128. Treating may comprise a process selected from the group including: exposing to vacuum, exposing to ultraviolet radiation, drying, heating, baking, rapid thermal processing, and annealing. Treatment in step 836 typically includes drying, rapid thermal processing ("RTP"), and annealing. Drying is typically

performed for one minute at 160°C, then at 260°C for four minutes. If used, the RTP is typically done at 725°C for 30 seconds, with a 100°C/sec. ramping rate. A furnace anneal, preferably in an oxygen atmosphere, crystallizes the metal oxide compound. Annealing is preferably conducted for 60 minutes at 800°C in oxygen flowing at 5 l/m, with 10 minutes "push" and 10 minutes "pull". Ferroelectric thin film 128 has a thickness in the range of from 5 nm to 500 nm, preferably from 30 nm to 100 nm.

In step 838, common plate top electrode layer 130, made of platinum and having a thickness of 100 nm, is deposited on ferroelectric thin film 128 using a conventional sputtering method. In step 840, common plate top electrode 130 and ferroelectric thin film 128 are patterned, removing from ILD 116 the portions above channel 109 and source 106 of MOSFET 114 to reduce interference with FGA processes. Common plate top electrode 130 and ferroelectric thin film 128 are patterned in step 840 so that they form stack capacitor 122, comprising bottom electrode 126 and ferroelectric thin film 128, and stack capacitor 222, comprising bottom electrode 226 and ferroelectric thin film 228.

In step 842, a final liquid MOD precursor for inventive hydrogen diffusion barrier layer 132 is prepared. Preferably, the precursor comprises tantalum 2-ethylhexanoate, suitable for forming Ta_2O_5 by application with the preferred LSMCD technique. A misted deposition method is preferred because the composition and deposition rate of the liquid precursor is more easily controlled than in alternative methods, thereby enabling formation of a very thin, uniform film of the barrier layer compound. In step 844, the wafer substrate is placed in a misted deposition reactor. Then a mist of the final precursor is formed and flowed into the deposition reactor, where the mist deposits, forming a liquid coating of the precursor on the common plate top electrode layer. In step 846, the liquid coating is treated to form hydrogen diffusion barrier layer 132 covering common plate top electrode 130 and ferroelectric thin film 128. Treating may comprise a process selected from the group including: exposing to vacuum, exposing to ultraviolet radiation, drying, heating, baking, rapid thermal processing, and annealing. Treatment in step 846 typically includes drying, rapid thermal processing ("RTP"), and annealing. Drying is typically performed for one minute at 160°C, then at 260°C for four minutes. If used, the RTP is typically done at 725°C for 30 seconds, with a 100°C/sec ramping rate. A furnace anneal,

preferably in an oxygen atmosphere, crystallizes the metal oxide compound. Annealing is preferably conducted for 60 minutes at 800°C in oxygen flowing at 5 l/m, with 10 minutes "push" and 10 minutes "pull". In step 848, hydrogen diffusion barrier layer 132 is patterned and etched from ILD 116 above channel 109 and source 106 of MOSFET 114 to reduce interference with FGA processes. Hydrogen diffusion barrier thin film 132 has a thickness in the range of from 5 nm to 500 nm, preferably from 30 nm to 100 nm. Thereafter, in step 850, memory cell 100 is completed using conventional techniques to form ILD 136 and passivation layer 142. Finally, hydrogen annealing is performed in step 852 to repair defects and restore desired semiconductor properties in the switch (MOSFET) 114. Preferably, the hydrogen anneal (FGA) of the integrated circuit is conducted at atmospheric pressure in a H_2-N_2 (forming gas) gas mixture with 1% to 5% H_2, at a temperature of between 200°C and 400°C for a time duration of from 10 to 40 minutes.

EXAMPLE 1

FIG. 11 is a diagrammatic cross-sectional view of an exemplary capacitor 900 having a hydrogen diffusion barrier layer fabricated in accordance with the invention.

A series of P-type 100 Si wafer substrates 902 were oxidized to form silicon dioxide layers 904. Each substrate 902 was dehydrated in a vacuum oven at 180°C for 30 minutes. Then a bottom platinum electrode layer 906 having a thickness of 300 nm was sputter-deposited on the substrate, using an argon atmosphere, 8 mTorr pressure and 0.53 amps. A dehydration bake was conducted in a vacuum oven at 180°C for 30 minutes. A 0.2 molar precursor solution containing strontium 2-ethylhexanoate, bismuth 2-ethylhexanoate and tantalum 2-ethylhexanoate in relative molar proportions corresponding to the stoichiometric formula $Sr_{0.9}Bi_{2.2}Ta_2O_9$ was diluted to 0.14 molar concentration using n-butyl acetate solvent. A dehydration bake was performed in a vacuum oven at 180°C for 30 minutes. A first spincoat of the 0.14 molar precursor solution was deposited on the bottom electrode at 1500 rpm for 30 seconds. This was baked using a hot plate for one minute at 160°C, then at 260°C for four minutes. A rapid thermal process (RTP) was performed in an oxygen atmosphere at 725°C for 30 seconds, with a ramping rate of 100°C/sec. The sequence of spin coating, baking and RTP was repeated. Each wafer was then annealed at 800°C for 60 minutes in O_2 gas flowing at 5 l/m, using a 10 minute push-

pull, to form a thin film of strontium bismuth tantalate ("SBT") layered superlattice material having a thickness of 190 nm.

Next, each wafer was dehydrated in a vacuum oven at 180°C for 30 minutes. Then platinum was sputter-deposited in an argon atmosphere at 8 mTorr pressure using 0.53 amps to make a top electrode layer 910 having 200 nm thickness. Top electrode layer 910, ferroelectric thin film 908 and bottom electrode 906 were patterned and etched in sequence to form individual capacitors 900 having a top surface area of approximately 400 square microns. Each wafer was then annealed at 700°C for 30 minutes in O_2 gas flowing at 5 l/m, using a 10 minute push-pull. In a group of the exemplary wafers, a hydrogen diffusion barrier layer 912 in accordance with the invention was formed to cover each capacitor 900, as depicted in FIG. 11. An initial precursor solution comprising tantalum 2-ethylhexanoate in xylenes solvent was diluted to 1.4 molar concentration with n-butyl acetate to make a final precursor for forming Ta_2O_5. The wafers containing the capacitors were given a dehydration bake in a vacuum oven at 180°C for 30 minutes. Then a first spin-on layer of the final precursor was applied at 2000 rpm for 30 seconds. The liquid coating was baked using a hot plate for one minute at 160°C, then at 260°C for four minutes. The sequence of spin coating and baking was repeated. Each wafer was then annealed at 700°C for 30 minutes in O_2 gas flowing at 5 l/m, using a 10 minute push-pull, to form a thin film 912 of Ta_2O_5 having a thickness of 40 nm.

Then ILD 914 was formed on all wafers using a conventional spin-on glass technique. A series of wiring holes 915 and wiring layers 916 were formed through ILD 914 and, if present, through hydrogen diffusion barrier layer 912 to allow electrical contact at surface portion 917 with top electrode 910. Finally, all wafers were given an oxygen anneal for 30 minutes at 450°C in O_2 gas flowing at 5 l/m using a 10 minute push-pull. The individual patterned capacitors typically had a surface area of about 400 square microns. The surface area ratio of surface portion 917 to the surface area of capacitor 900 corresponded to the ratio typically found in integrated circuit memory capacitors.

Hysteresis curves of the $Sr_{0.9}Bi_{2.2}Ta_2O_9$ ("SBT") capacitors, both with and without a hydrogen diffusion barrier layer, were measured. Then all capacitors were given a FGA treatment at 450°C for 30 minutes in a H_2/N_2 atmosphere having 5% H_2.

After the FGA treatment, the ferroelectric properties of the thin films of the capacitors were measured again. The measurements were performed on about 20 individual capacitors selected from about five different wafers, and the effect of FGA on polarizabilty was studied by comparing the hysteresis curves of capacitors with and without a hydrogen diffusion barrier layer. Representative results are presented in FIGS. 12 and 13. FIG. 12 is a graph of hysteresis curves measured before and after FGA, in which polarization, $\mu C/cm^2$, is plotted as a function of electric field, in units of kV/cm, in a SBT thin-film capacitor having no hydrogen diffusion barrier layer. FIG. 13 is a graph of hysteresis curves measured before and after FGA, in which polarization, $\mu C/cm^2$, is plotted as a function of electric field, in units of kV/cm, in a SBT thin-film capacitor having an inventive hydrogen diffusion barrier layer. The graph of FIG. 12 shows that the remanent polarization in the SBT capacitor having no inventive hydrogen diffusion barrier layer decreases from about 18 $\mu C/cm^2$ before FGA to about 10 $\mu C/cm^2$ after FGA. "Remanent polarization" is the 2Pr value, which is the absolute value measured from the hysteresis curve in the vertical direction at the value of zero on the horizontal axis. For practical commercial integrated circuit nonvolatile memory applications, a value of remanent polarization of about 12 $\mu C/cm^2$ is typically required. Thus, without the barrier layer, the polarization was reduced so much that the material would not be practical for a commercial memory. The graph of FIG. 13 shows that the SBT capacitor covered by a hydrogen diffusion barrier layer according to the invention does not suffer a perceptible decline in remanent polarization as a result of FGA. The 2Pr-value remains about 18 $\mu C/cm^2$ after FGA, well above the value necessary for a practical memory.

There has been described new compositions of hydrogen diffusion barrier layers for protecting both ferroelectric and nonferroelectric, high-dielectric constant metal oxide materials in integrated circuits against hydrogen degradation. Also, there has been described a method and structures for fabricating ferroelectric and dielectric integrated circuits that permit exposure to hydrogen and still result in devices with good electronic properties. It should be understood that the particular embodiments shown in the drawings and described within this specification are for purposes of example and should not be construed to limit the invention which will be described in the claims below. Further, it is evident that those skilled in the art may now make

numerous uses and modifications of the specific embodiments described, without departing from the inventive concepts. It is also evident that the steps recited may in some instances be performed in a different order; or equivalent structures and processes may be substituted for the various structures and processes described.

WE CLAIM:

1. An integrated circuit (100, 200, 300, 400, 500, 700, 740, 900) comprising:

a dielectric thin film (128, 328, 428, 528, 711, 764, 908) of metal oxide material; and

a hydrogen diffusion barrier layer (132, 332, 432, 532, 720, 750, 770, 912), said hydrogen diffusion barrier layer located to inhibit the diffusion of hydrogen towards said dielectric thin film, and said hydrogen diffusion barrier layer comprising an oxide selected from the group consisting of tantalum pentoxide, aluminum oxide, tungsten oxide and titanium oxide.

2. An integrated circuit as in claim 1 wherein said hydrogen diffusion barrier layer comprises a metal oxide selected from the group consisting of Ta_2O_5, WO_3, Al_2O_3, and TiO_2.

3. An integrated circuit as in claim 1 wherein said hydrogen diffusion barrier layer comprises Ta_2O_5.

4. An integrated circuit as in claim 1 wherein a portion of said hydrogen diffusion barrier layer is located directly over at least a portion of said dielectric thin film.

5. An integrated circuit as in claim 1 wherein a portion of said hydrogen diffusion barrier layer is located laterally from said dielectric thin film.

6. An integrated circuit as in claim 1 wherein said dielectric thin film has a side portion and said hydrogen diffusion barrier layer covers said side portion.

7. An integrated circuit as in claim 1 wherein said dielectric thin film comprises ferroelectric material.

8. A ferroelectric FET as in claim 7 wherein said ferroelectric material comprises an ABO_3-type perovskite.

9. An integrated circuit as in claim 7 wherein said ferroelectric material comprises layered superlattice material.

10. An integrated circuit as in claim 9 wherein said layered superlattice material comprises strontium, bismuth and tantalum.

11. An integrated circuit as in claim 9 wherein said layered superlattice material comprises strontium, bismuth, tantalum and niobium in relative molar proportions corresponding to a stoichiometric formula $Sr_aBi_b(Ta_cNb_d)O_{[9+(a-1)+(b-2)(1.5)]}$, where $0.9 \leq a \leq 1$,

$2 \leq b \leq 2.2$, and $(c+d)=2$.

12. An integrated circuit as in claim 11 wherein $d=0$.

13. An integrated circuit as in claim 11 wherein $d=0.5$.

14. An integrated circuit as in claim 1 wherein said dielectric thin film comprises nonferroelectric, high-dielectric constant material.

15. An integrated circuit as in claim 14 wherein said dielectric thin film comprises layered superlattice material.

16. An integrated circuit as in claim 1, further comprising a bottom electrode and a top electrode, said dielectric thin film disposed between said bottom electrode and said top electrode, wherein said hydrogen diffusion barrier layer is located directly over said top electrode.

17. An integrated circuit as in claim 16, further comprising a lower diffusion barrier layer, said lower diffusion barrier layer disposed under said bottom electrode.

18. An integrated circuit as in claim 17 wherein said lower diffusion barrier layer comprises a metal oxide.

19. An integrated circuit as in claim 18 wherein said lower diffusion barrier layer comprises IrO_2.

20. An integrated circuit as in claim 18 wherein said lower diffusion barrier layer comprises an oxide selected from the group consisting of tantalum pentoxide, aluminum oxide, tungsten oxide and titanium oxide.

21. An integrated circuit as in claim 1, further comprising a semiconductor substrate, a channel region in said semiconductor substrate, and a gate electrode, wherein said dielectric thin film comprises ferroelectric material and is located directly above said channel region, and said gate electrode is above said dielectric thin film.

22. An integrated circuit as in claim 21 wherein said dielectric thin film is included in a ferroelectric FET memory.

23. An integrated circuit as in claim 21 wherein said hydrogen diffusion barrier layer comprises a metal oxide selected from the group consisting of Ta_2O_5, WO_3, Al_2O_3, and TiO_2.

24. An integrated circuit as in claim 21 wherein said hydrogen diffusion barrier layer comprises Ta_2O_5.

25. An integrated circuit as in claim 21 wherein a portion of said hydrogen

diffusion barrier layer is located directly over at least a portion of said dielectric thin film.

26. An integrated circuit as in claim 21 wherein a portion of said hydrogen diffusion barrier layer is located laterally from said dielectric thin film.

27. An integrated circuit as in claim 21 wherein said dielectric thin film has a side portion and said hydrogen diffusion barrier layer covers said side portion.

28. A ferroelectric FET as in claim 21 wherein said ferroelectric material comprises an ABO_3-type perovskite.

29. An integrated circuit as in claim 21 wherein said ferroelectric material comprises layered superlattice material.

30. An integrated circuit as in claim 29 wherein said layered superlattice material comprises strontium, bismuth and tantalum.

31. An integrated circuit as in claim 30 wherein said layered superlattice material comprises strontium, bismuth, tantalum and niobium in relative molar proportions corresponding to a stoichiometric formula $Sr_aBi_b(Ta_cNb_d)O_{[9+(a-1)+(b-2)(1.5)]}$, where $0.9 \leq a \leq 1$, $2 \leq b \leq 2.2$, and $(c+d)=2$.

32. An integrated circuit as in claim 21, further comprising a doped region in said semiconductor substrate, wherein said hydrogen diffusion barrier layer is not directly above said doped region.

33. An integrated circuit as in claim 21, further comprising a gate insulating layer, said gate insulating layer located between said dielectric thin film and said channel region.

34. An integrated circuit as in claim 33 wherein said gate insulating layer comprises an oxide selected from the group consisting of tantalum pentoxide, aluminum oxide, tungsten oxide and titanium oxide.

35. An integrated circuit comprising:

a first electronic element having electrical properties which improve when exposed to a reducing process;

a second electronic element having electrical properties which degrade when exposed to a reducing process;

a non-conducting reducing process barrier layer, said non-conducting barrier layer completely overlying said second element to protect it from said reducing

process while leaving said first element exposed to said reducing process.

36. An integrated circuit as in claim 35 wherein said first electronic element is a transistor.

37. An integrated circuit as in claim 35 wherein said second electronic element is a capacitor.

38. An integrated circuit as in claim 37 wherein said integrated circuit includes a plurality of said capacitors, each of said capacitors having a dielectric layer and a top electrode overlying said dielectric layer, said top electrodes being formed by a single, continuous common conducting layer common to said plurality of capacitors.

39. An integrated circuit as in claim 38 wherein said dielectric layers in each of said capacitors are formed by a single, continuous dielectric layer common to said plurality of capacitors.

40. An integrated circuit as in claim 38 wherein said first electronic element is a transistor, there are a plurality of said transistors, each of said transistors associated with one of said plurality of capacitors, and each of said capacitors is displaced laterally from its associated transistor so that it is not located directly over any portion of said transistor.

41. An integrated circuit as in claim 37 wherein said first electronic element is a transistor and said capacitor is displaced laterally from said transistor so that it is not located directly over any portion of said transistor.

42. An integrated circuit as in claim 37 wherein said capacitor has a side portion and said non-conducting reducing process barrier layer is further located laterally of said side portion.

43. An integrated circuit as in claim 35 wherein said barrier layer comprises an oxide selected from the group consisting of tantalum pentoxide, aluminum oxide, tungsten oxide and titanium oxide

44. An integrated circuit as in claim 35 wherein said second electronic element comprises a ferroelectric material.

45. A ferroelectric FET as in claim 44 wherein said ferroelectric material comprises an ABO_3-type perovskite.

46. An integrated circuit as in claim 44 wherein said ferroelectric material comprises layered superlattice material.

47. An integrated circuit as in claim 46 wherein said layered superlattice material comprises strontium, bismuth and tantalum.

48. An integrated circuit as in claim 46 wherein said layered superlattice material comprises strontium, bismuth, tantalum and niobium in relative molar proportions corresponding to a stoichiometric formula $Sr_aBi_b(Ta_cNb_d)O_{[9+(a-1)+(b-2)(1.5)]}$, where $0.9 \leq a \leq 1$, $2 \leq b \leq 2.2$, and $(c+d)=2$.

49. An integrated circuit as in claim 48 wherein $d=0$.

50. An integrated circuit as in claim 48 wherein $d=0.5$.

51. An integrated circuit as in claim 35 wherein said second electronic element comprises a nonferroelectric, high-dielectric constant material.

52. An integrated circuit as in claim 51 wherein said nonferroelectric, high-dielectric constant material comprises a material selected from the group consisting of layered superlattice materials and ABO_3-type perovskite materials.

53. An integrated circuit comprising:

a bottom electrode;

a common plate top electrode;

a dielectric thin film disposed between said bottom electrode and said common plate top electrode; and

a hydrogen diffusion barrier layer, said hydrogen diffusion barrier layer completely overlying said dielectric thin film.

54. An integrated circuit as in claim 53 wherein said hydrogen diffusion barrier layer is further located laterally from said dielectric thin film.

55. An integrated circuit as in claim 53, further comprising a lower diffusion barrier layer, said lower diffusion barrier layer disposed under said bottom electrode.

56. An integrated circuit as in claim 53, further comprising a plurality of bottom electrodes, said dielectric thin film disposed between said bottom electrodes and said common plate top electrode.

57. An integrated circuit as in claim 56 wherein said dielectric thin film has a plurality of capacitor portions, each of said capacitor portions located between one of said bottom electrodes and said common plate top electrode, and wherein said hydrogen diffusion barrier layer completely overlies over each of said capacitor portions.

58. An integrated circuit as in claim 57 wherein said hydrogen diffusion barrier is continuous over each of said capacitor portions.

59. An integrated circuit as in claim 58, further comprising a plurality of lower diffusion barrier layers, wherein said lower diffusion barrier layers are disposed under said bottom electrodes.

60. An integrated circuit comprising:

a bottom electrode;

a top electrode;

a dielectric thin film disposed between said bottom electrode and top electrode; and

a diffusion barrier layer, said diffusion barrier layer underlying said dielectric thin film, said diffusion barrier layer comprising an oxide selected from the group consisting of tantalum pentoxide, aluminum oxide, tungsten oxide, titanium oxide and iridium oxide.

61. An integrated circuit as in claim 60 wherein said diffusion barrier layer comprises a metal oxide selected from the group consisting of Ta_2O_5, WO_3, Al_2O_3, TiO_2, and IrO_2.

62. An integrated circuit as in claim 60 wherein said diffusion barrier layer comprises Ta_2O_5.

63. An integrated circuit as in claim 60 wherein said diffusion barrier layer underlies said bottom electrode.

64. A method of fabricating an integrated circuit comprising steps of:

providing a substrate;

forming a dielectric thin film; and

forming a hydrogen diffusion barrier layer, said hydrogen diffusion barrier layer located to inhibit the diffusion of hydrogen towards said dielectric thin film, and said hydrogen diffusion barrier layer comprising an oxide selected from the group consisting of tantalum pentoxide, aluminum oxide, tungsten oxide and titanium oxide.

65. A method of fabricating an integrated circuit as in claim 64 wherein said step of forming a hydrogen diffusion barrier layer comprises:

providing a liquid precursor of said hydrogen diffusion barrier layer; and

utilizing said liquid precursor to form said hydrogen diffusion barrier layer.

66. A method of fabricating an integrated circuit as in claim 65 wherein said step of utilizing said liquid precursor comprises: applying said liquid precursor to said substrate; and treating said substrate to form said hydrogen diffusion barrier layer.

67. A method of fabricating an integrated circuit as in claim 66 wherein said applying said liquid precursor includes: forming a mist of said liquid precursor; and depositing said mist on said substrate in a liquid coating.

68. A method as in claim 66 wherein said step of treating comprises a process selected from the group consisting of: exposing to vacuum, exposing to ultraviolet radiation, drying, heating, baking, rapid thermal processing, and annealing.

69. A method of fabricating an integrated circuit as in claim 65 wherein said liquid precursor comprises a metal organic precursor compound selected from the group consisting of metal beta-diketonates, metal polyalkoxides, metal dipivaloylmethanates, metal cyclopentadienyls, metal alkoxycarboxylates, metal carboxylates, metal alkoxides, metal ethylhexanoates, metal octanoates, and metal neodecanoates.

70. A method of fabricating an integrated circuit as in claim 69 wherein said liquid precursor comprises a metal 2-ethylhexanoate.

71. A method of fabricating an integrated circuit as in claim 70 wherein said liquid precursor comprises a compound selected from the group consisting of tantalum 2-ethylhexanoate, tungsten 2-ethylhexanoate, and aluminum 2-ethylhexanoate.

72. A method of fabricating an integrated circuit comprising steps of: providing a substrate; forming a diffusion barrier layer; and forming a dielectric thin film over said diffusion barrier layer; wherein said step of forming a diffusion barrier layer comprises:

providing a liquid precursor of said lower diffusion barrier layer;

forming a mist of said liquid precursor and depositing said mist on said substrate; and

treating said mist to form said diffusion barrier layer.

73. A method of fabricating an integrated circuit as in claim 72 wherein said liquid precursor contains a metal organic precursor compound selected from the group consisting of metal beta-diketonates, metal polyalkoxides, metal dipivaloylmethanates, metal cyclopentadienyls, metal alkoxycarboxylates, metal carboxylates, metal alkoxides, metal ethylhexanoates, metal octanoates, and metal neodecanoates.

74. A method of fabricating an integrated circuit as in claim 72 wherein said liquid precursor contains a metal organic precursor compound suitable for forming IrO_2.

75. A method of fabricating an integrated circuit as in claim 74 wherein said liquid precursor contains iridium 2-ethylhexanoate.

76. A method of fabricating an integrated circuit comprising steps of: providing a substrate; forming a diffusion barrier layer comprising iridium oxide; and forming a dielectric thin film; wherein said step of forming a diffusion barrier layer comprises:

providing a liquid precursor for iridium oxide;

utilizing said liquid precursor to form said diffusion barrier layer.

77. A method of fabricating an integrated circuit as in claim 76 wherein said liquid precursor contains a metal organic precursor compound selected from the group consisting of iridium beta-diketonates, iridium polyalkoxides, iridium dipivaloylmethanates, iridium cyclopentadienyls, iridium alkoxycarboxylates, iridium carboxylates, iridium alkoxides, iridium ethylhexanoates, iridium octanoates, and iridium neodecanoates.

78. A method of fabricating an integrated circuit as in claim 77 wherein said liquid precursor comprises iridium 2-ethylhexanoate.

79. A method of fabricating an integrated circuit as in claim 75 wherein said liquid precursor comprises an organic precursor compound suitable for forming IrO_2.

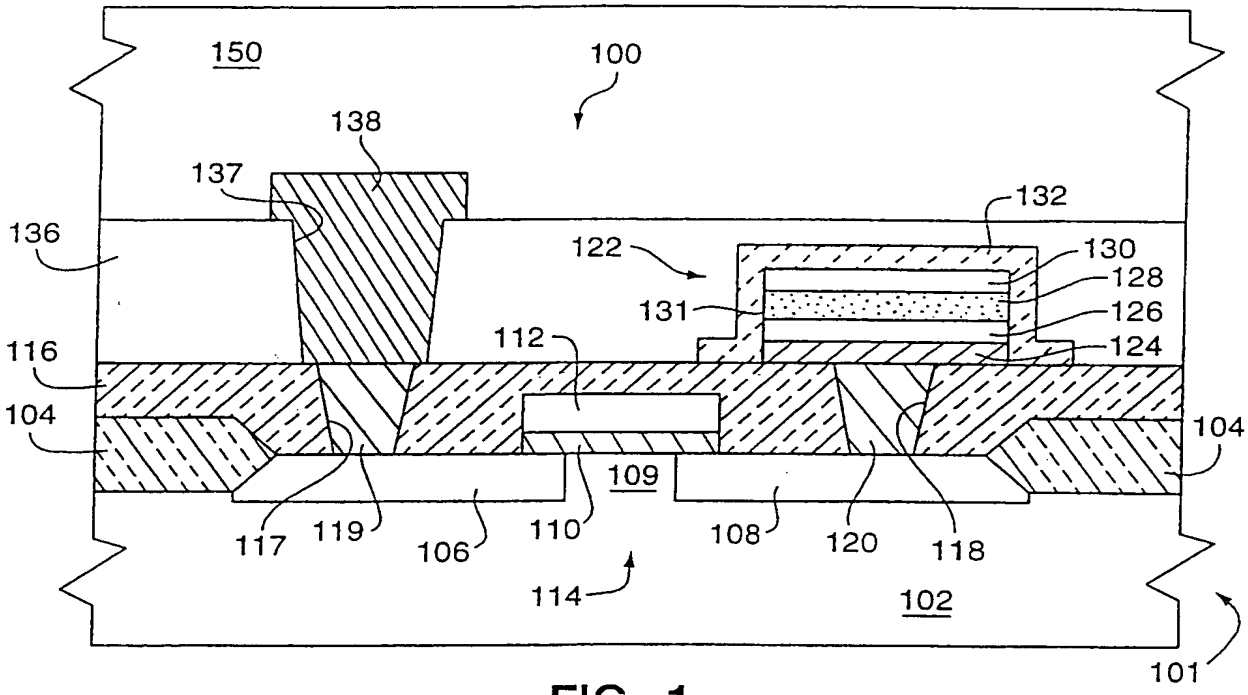
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FIG. 1

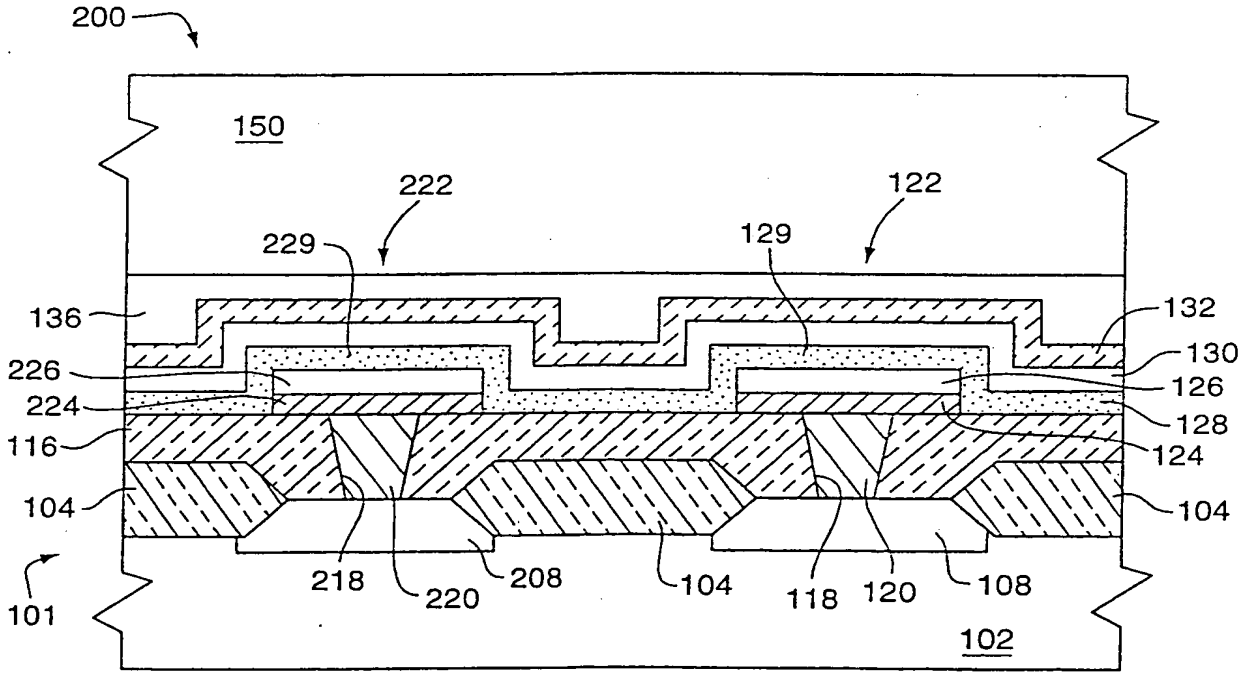
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FIG. 2

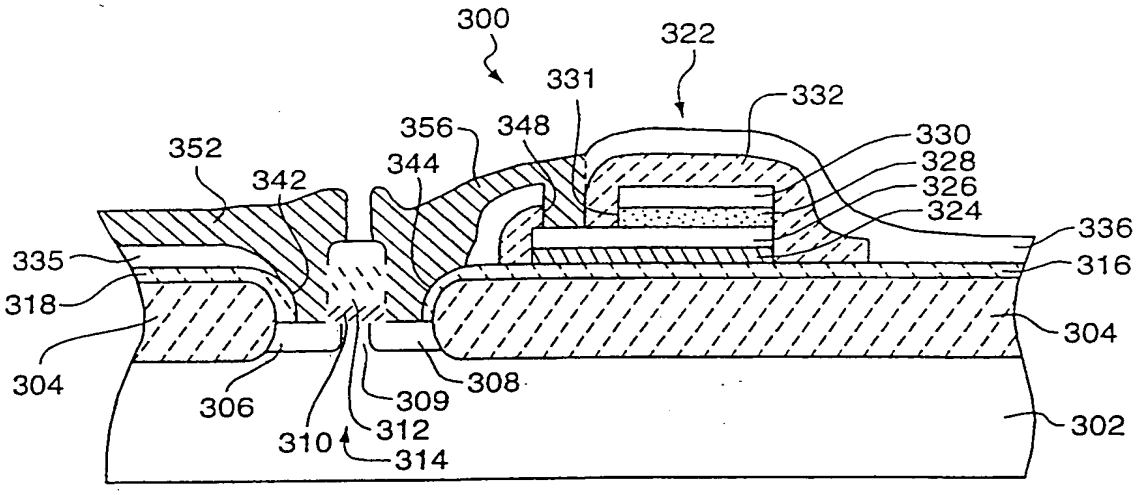
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FIG. 3

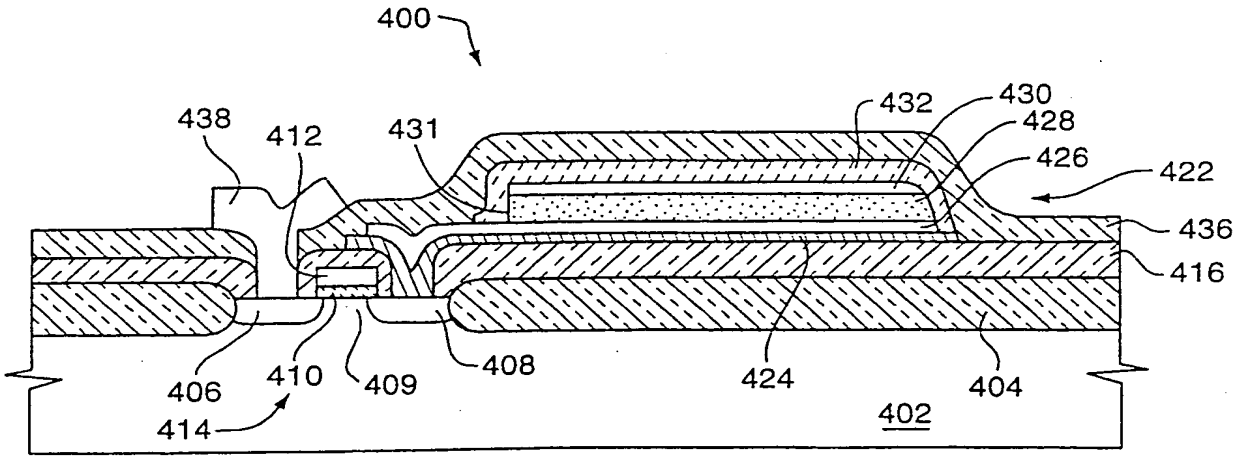
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FIG. 4

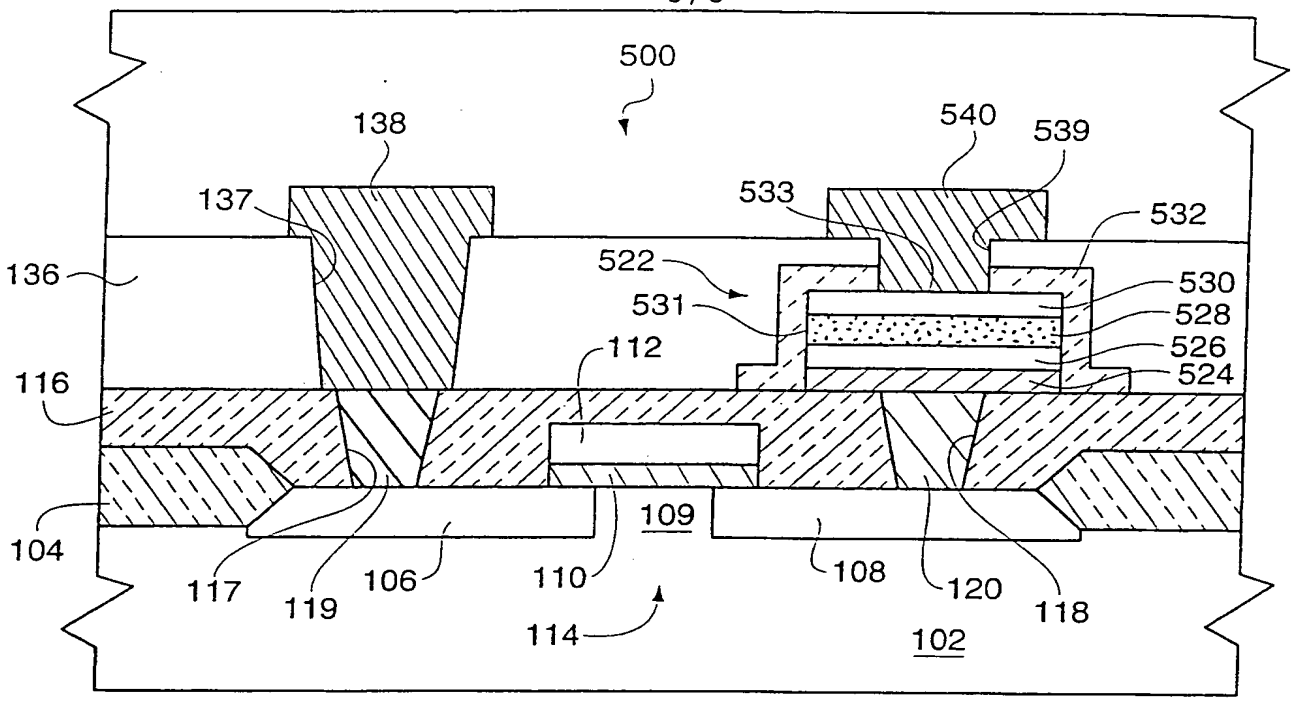


FIG. 5

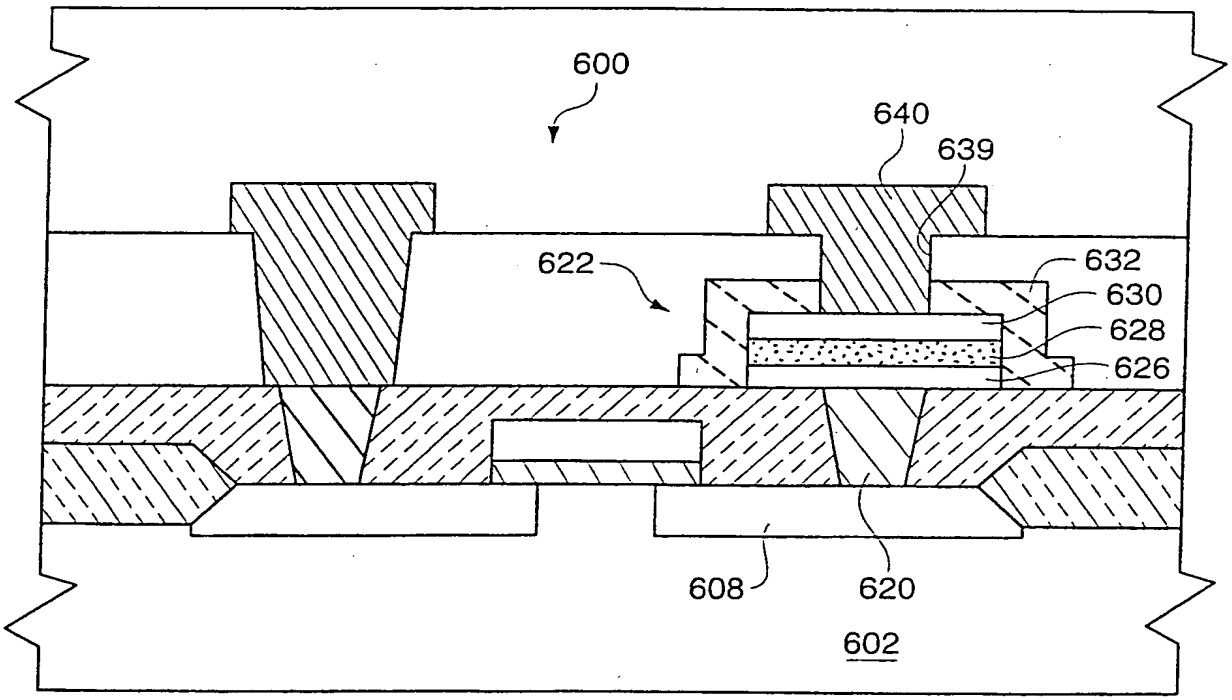


FIG. 6
PRIOR ART

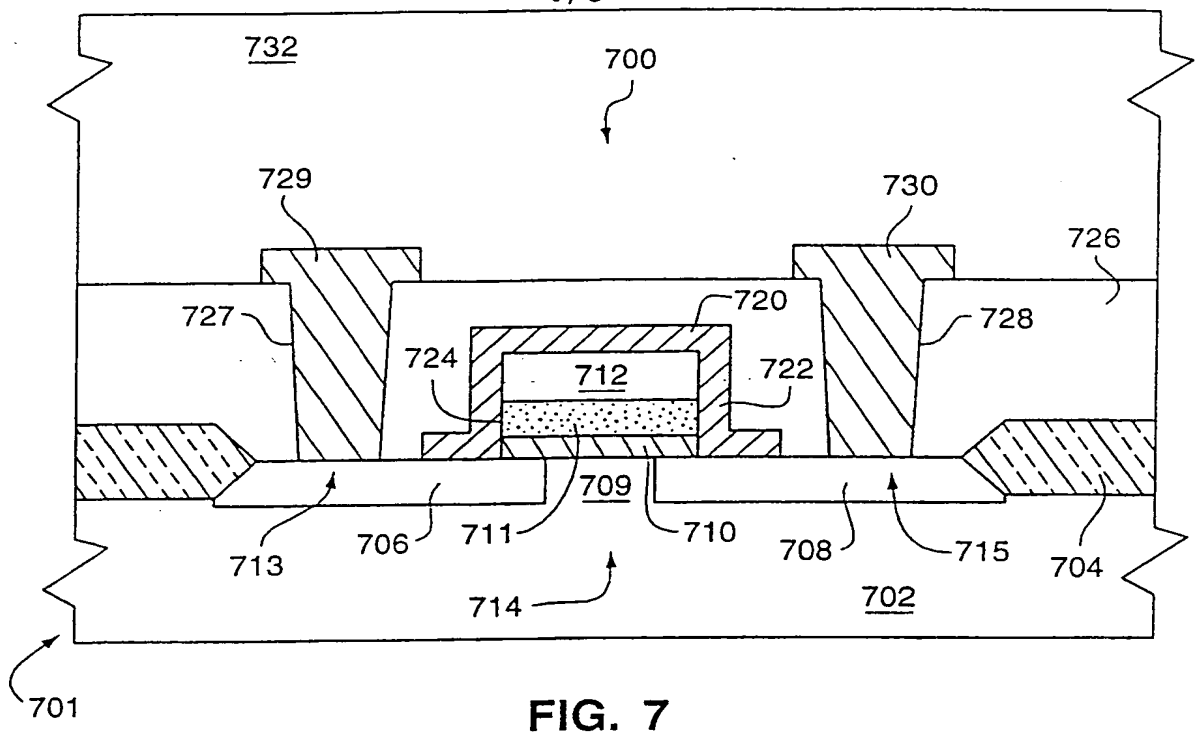


FIG. 7

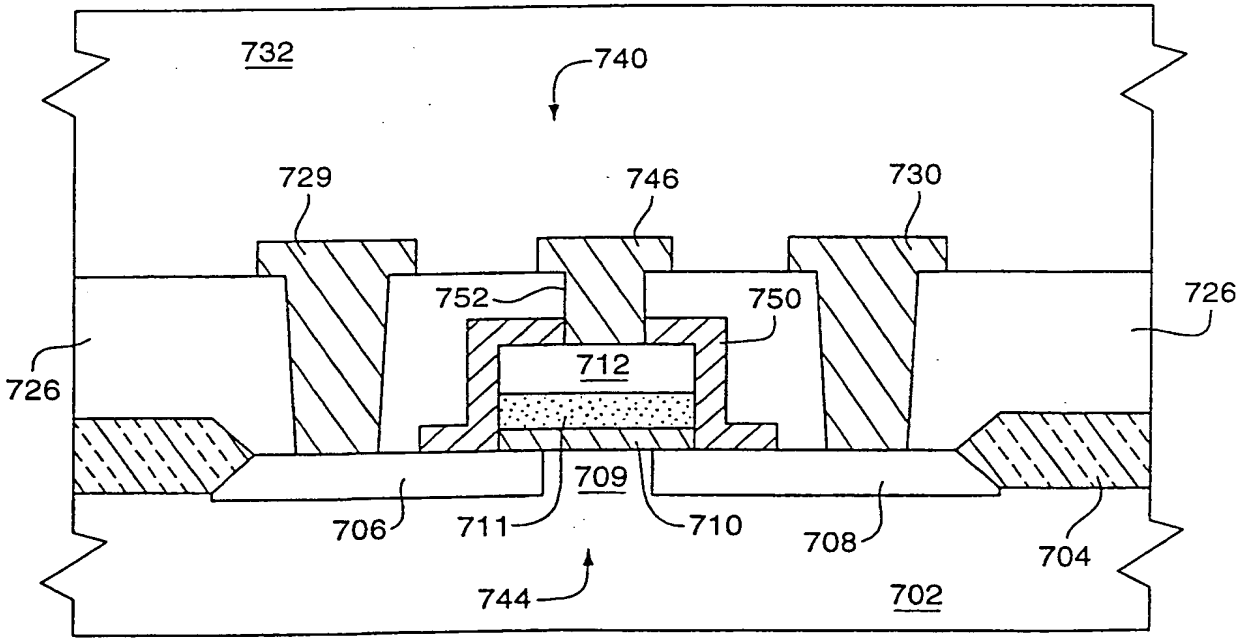


FIG. 8

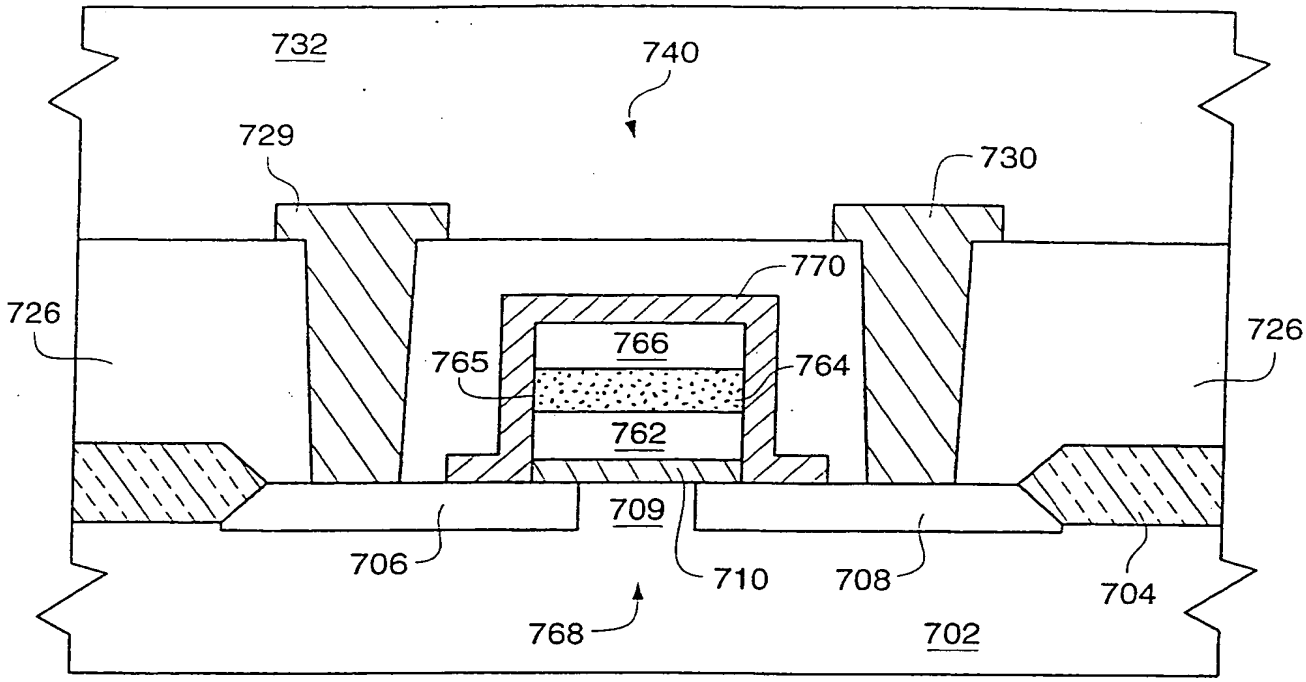


FIG. 9

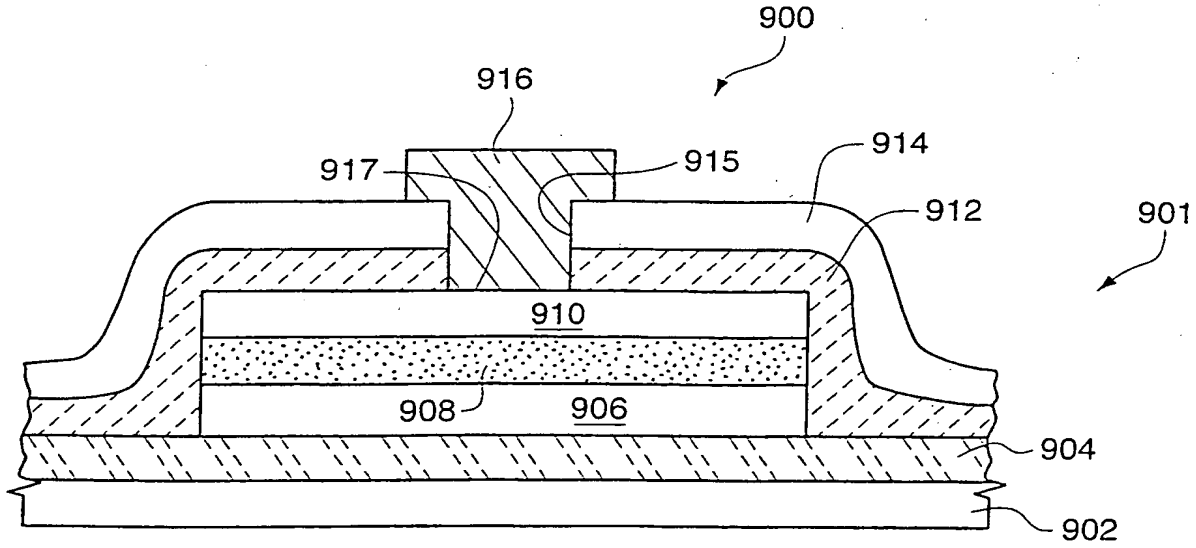
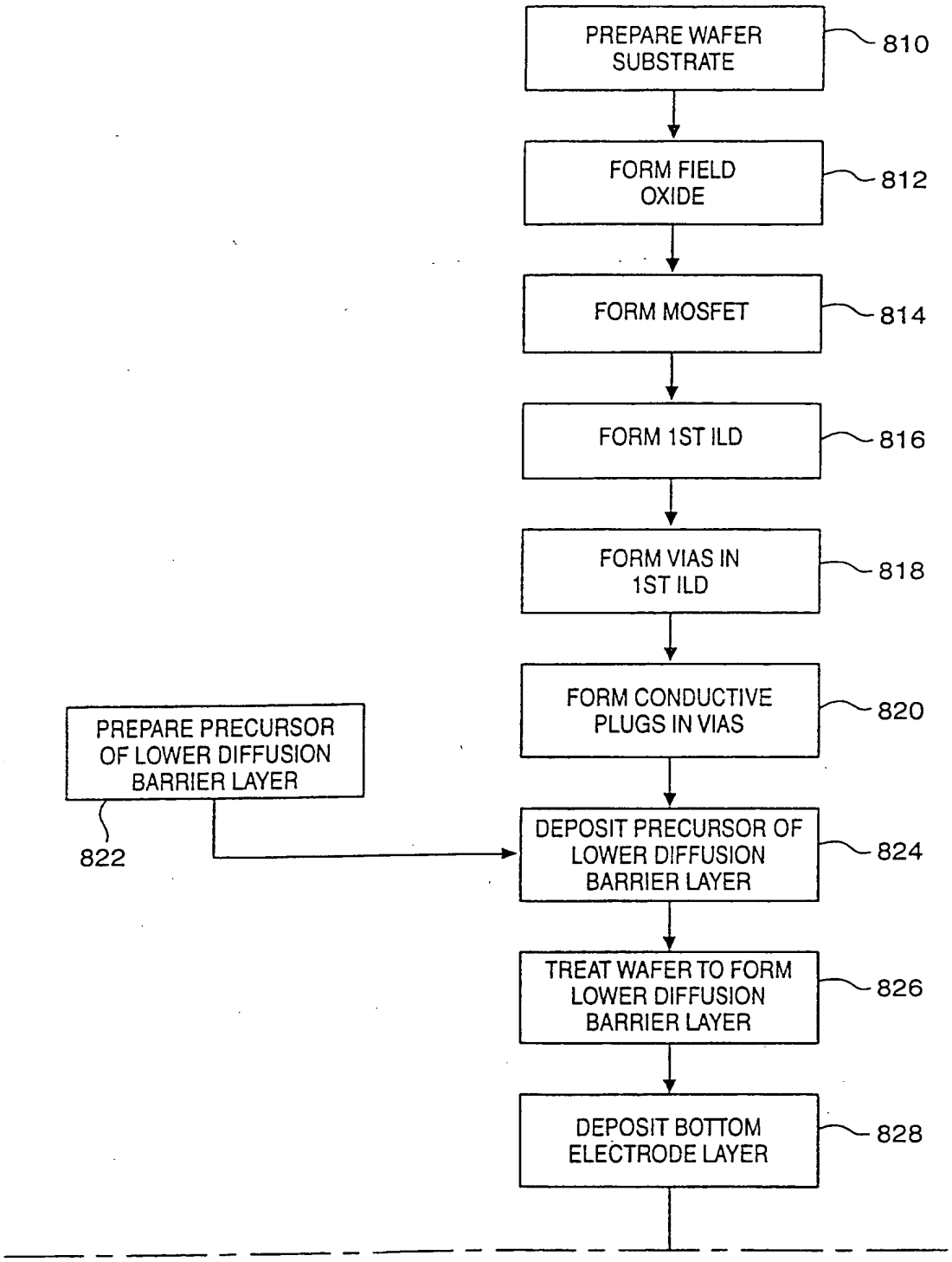


FIG. 11

FIG. 10A


PREPARE WAFER SUBSTRATE
810
FORM FIELD OXIDE
812
FORM MOSFET
814
FORM 1ST ILD
816
FORM VIAS IN 1ST ILD
818
FORM CONDUCTIVE PLUGS IN VIAS
820
PREPARE PRECURSOR OF LOWER DIFFUSION BARRIER LAYER
822
DEPOSIT PRECURSOR OF LOWER DIFFUSION BARRIER LAYER
824
TREAT WAFER TO FORM LOWER DIFFUSION BARRIER LAYER
826
DEPOSIT BOTTOM ELECTRODE LAYER
828

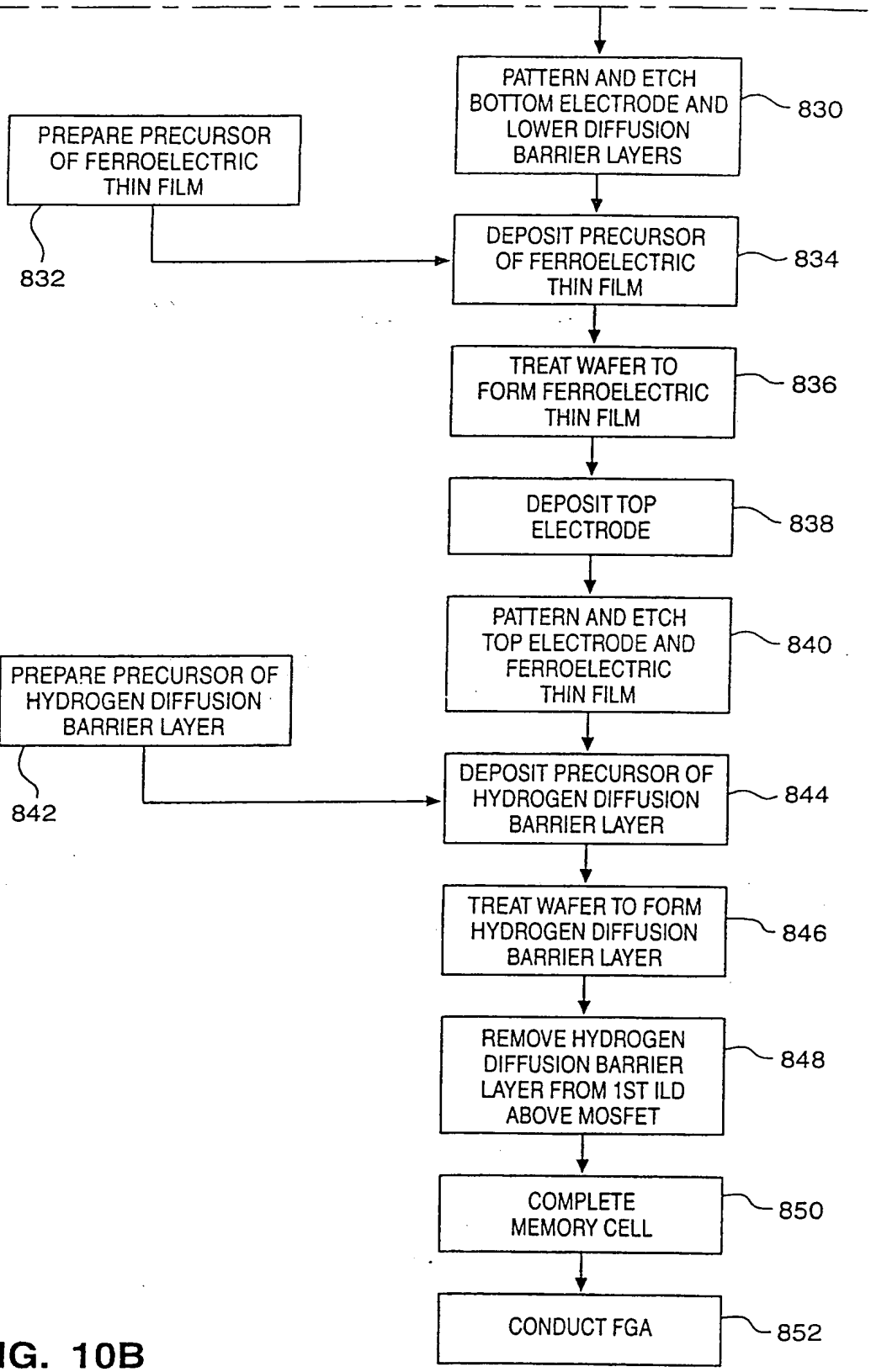

PATTERN AND ETCH BOTTOM ELECTRODE AND LOWER DIFFUSION BARRIER LAYERS
830
PREPARE PRECURSOR OF FERROELECTRIC THIN FILM
832
DEPOSIT PRECURSOR OF FERROELECTRIC THIN FILM
834
TREAT WAFER TO FORM FERROELECTRIC THIN FILM
836
DEPOSIT TOP ELECTRODE
838
PATTERN AND ETCH TOP ELECTRODE AND FERROELECTRIC THIN FILM
840
PREPARE PRECURSOR OF HYDROGEN DIFFUSION BARRIER LAYER
842
DEPOSIT PRECURSOR OF HYDROGEN DIFFUSION BARRIER LAYER
844
TREAT WAFER TO FORM HYDROGEN DIFFUSION BARRIER LAYER
846
REMOVE HYDROGEN DIFFUSION BARRIER LAYER FROM 1ST ILD ABOVE MOSFET
848
COMPLETE MEMORY CELL
850
CONDUCT FGA
852

FIG. 10B

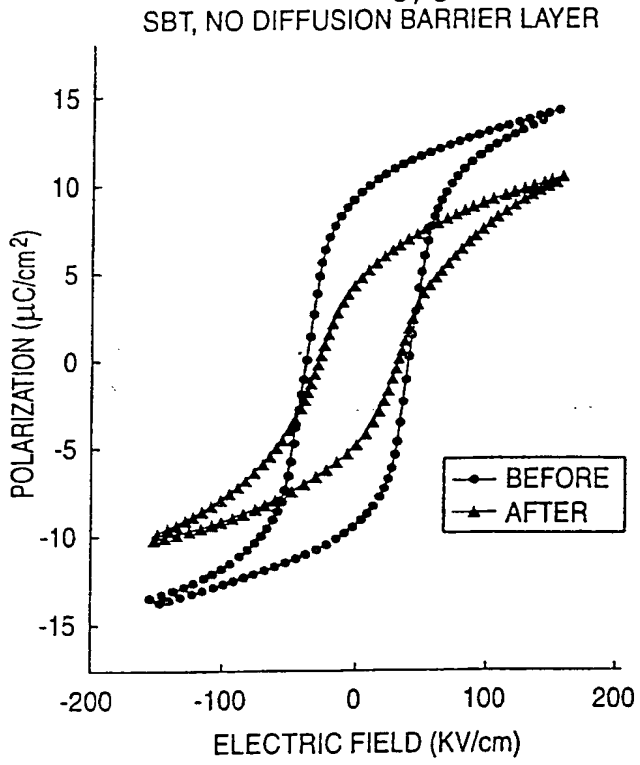


FIG. 12

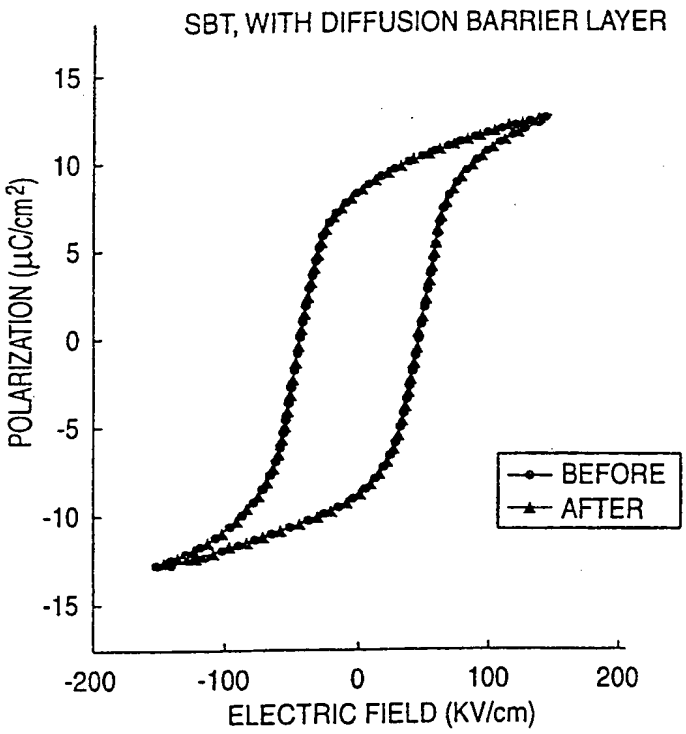


FIG. 13

INTERNATIONAL SEARCH REPORT

Ir. ational Application No
PCT/US 00/24993

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/02 H01L29/51 H01L27/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IN SEON PARK ET AL: "ULTRA-THIN EBL (ENCAPSULATED BARRIER LAYER) FOR FERROELECTRIC CAPACITOR" INTERNATIONAL ELECTRON DEVICES MEETING,US,NEW YORK, NY: IEEE, 7 December 1997 (1997-12-07), pages 617-620, XP000855872 ISBN: 0-7803-4101-5 the whole document ---	1,2,5-9, 16, 53-55, 60,61,63
X	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 02, 30 January 1998 (1998-01-30) & JP 09 260516 A (SHARP CORP), 3 October 1997 (1997-10-03) abstract ---	1,2,4,7, 53
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 February 2001	08/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Baillet, B

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INTERNATIONAL SEARCH REPORT

Ir. .ational Application No
PCT/US 00/24993

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	abstract	19
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